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Power Efficient 14T Full Adder with Body Biasing Technique

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Abstract*—Leakage power reduction is the major issue in digital circuits. Many techniques are applied to reduce leakage power. In this paper one such technique Body Biasing is used to design the Full adder. It is very efficient techniques to decrease leakage power or static power. The results express that it has not only reduced the static power but has also proven efficient in decreasing the dynamic power (Power Consumption).*

The conventional 14T full adder employing 14 transistors is redesigned using Body Biasing. Then both transistors are compared on the basis of different parameters Average power (dynamic power), Average Delay, Average leakage power (Static Power). We found that after body biasing the average and leakage power has reduced effectively.

The source voltage for both the circuits is same i.e. 0.7V and the bias voltage in modified 14T Full adder is also 0.7V. Cadence VIRTUOSO tool has been used for making schematics on 45nm BSIM3 is used for carrying out simulations.

Keywords:— *Body Biasing, Average Power, Leakage Power, Average Delay.*

1. INTRODUCTION

The complication of circuits rises with the growing demand of wireless devices. complexity denotes the much amount of transistors on single chip. As many components are increasing, power consumption is also increasing rapidly.

CMOS (Complementary metal oxide semiconductor) is most popular among designing of all modern digital logic circuits. Reduction of power depletion and leakage power remains a key challenge for the researchers. Here power can be classified as dynamic power (power consumption) and leakage power [12]. Due to growth in CMOS technology size and threshold voltage is scaling down continuously, and this in turn results in increment of leakage power exponentially. Body biasing can be used to lessen the power consumption and leakage power effectively. Basically in body biasing we connect the MOSFET terminal i.e. 4^{th} terminal to the potential. Body effect takes place when the substrate of transistor is not connected at same level as that of source [13]. Body biasing changes a threshold voltage of device. The extremely crucial parameter which will have to be regarded at the similar time designing any device is the power dissipation.

VLSI (Very Large-Scale Integration) works on both digital and analog. In Digital applications, the scaling of the gate delay and power dissipation is of interest.

2. CONVENTIONAL FULL ADDER

It is a combinational circuit which sums three bits and provides outputs as carry and sum. All electronic devices contains

Microchips, and Digital Signal Processors. All of these devices use operation of addition [3]. Thus adders play a significant role in performance of whole circuit and effective implementation of adder in circuits is very important. Thus the reduction in leakage power and power depletion of full adder will result in enhancement of performance of whole circuitry.

The outputs of full adder can be calculated as:

$$\text{Sum} = (\text{A xor B}) \text{ xor } C_{in}$$

$$\text{Carry} = \text{A and B} + C_{in} \ (\text{A xor B})$$

Here A, B and Cin are inputs and Carry and Sum are outputs.

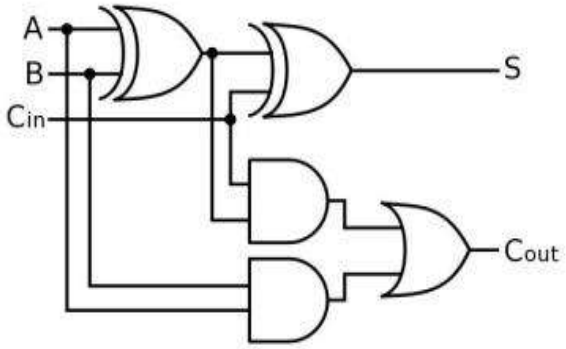

Figure 1: Block Diagram of Full Adder

Table 1. Truth Table of 1-Bit Full Adder

Input			Output	
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full adder can be designed by different logic ways. Each logic style has different number of transistors. Many researchers have presented number of full adder employing different logic style. Most popular among those are conventional 28 transistor full adder, TGA (Transmission gate Adder) 20T full adder, 9A, 9B, 13A, 14T full adder, GDI based 10T full adder, SERF based 10T full adder and many more. The analysis of these adders shows that GDI based full adders have low average power. The TG depending full adders performs well in case of Average Delay. Although the PDP (power delay product) is low for 14T Full adder but its Power Dissipation (Leakage Power) is low.

In this paper the conventional 14T full adder is intended with Body biasing in order to modify the circuit and enhance the performance. The purpose of applying body biasing to the adder is to decline the leakage power and power consumption.

3. 14T FULL ADDER

It is a one of the most efficient adders used these days. 14T full adder as shown in fig.2. It has been found during evaluation it tick marks all the boxes of speed, power consumption, delay, etc. In terms of simplicity it less complex than that of conventional adder. It also consumes lesser power than conventional full adder, less delay. Ideally it is a better than conventional 28T Full adder in terms of power consumption, delay, leakage power and also chip size is reduced due to reduction in transistor count. It has 4 transistors XOR that are inverted in the next phase to generate XNOR [9]. These XNOR and XOR are utilized instantaneously to produce Cout and Sum [9].

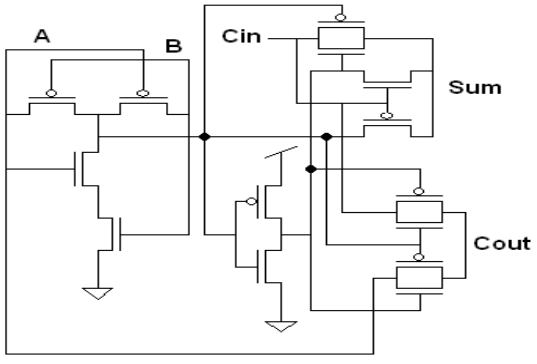

Figure 2: Conventional 14T Full Adder

4. BODY BIASING

It is a method in which the substrate are biased to something else then GND in case of NMOS or Vdd in case of PMOS. This technique is very efficient in reducing leakage power (Static Power). It affects less on dynamic power. Body biasing gives impressive results down to 65nm because at < 65nm the channel leakage is the highest static power contributor. Body Bias is the voltage at which the terminal (4^{th} terminal of MOSFET) is connected. In the present work the 14T full adder is designed by body biasing. The 4^{th} terminal of transistors is connected to the Vdc and in case of PMOS the highest voltage is given is 0.7V and in case of NMOS the voltage 0V.

Being most efficient 14T adder became the first choice to do the modifications. As mentioned above Body Biasing seems to be very effect technique to work with. Hence the 14T Full adder circuit is simulated with body biasing in order to enhance its performance and compare the results. Cadence VIRTUOSO tool has been used for making schematics on 45nm BSIM3 is used for carrying out simulations. Performance of adders are compered on the basis of Average Power, Average Delay, Leakage Power

5. RESULT AND SIMULATION

The simulation of 14T full adder and modified 14T full adder employing Body Biasing is obtained and compared. The simulation is performed by Cadence Virtuoso which works at 45nm. The comparison is done on the basis of Average delay and Leakage power. The supply voltage and the bias voltage are 0.7V.

Average Power

It is informative to go back to basics and examine what we mean by average power and why we are even concerned in them. The instantaneous power $P(t)$ consumed or supplied by a circuit component is the multiply of the current through the component and the voltage across the component [11]

$$P(t) = I(t)V(t)$$

The energy consumed or supplied over some time interval T is the integral of the instant power [11]

$$E = \int_0^T P(t)dt$$

The average power over this interval is

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T P(t)dt$$

Table 2: Average Power in 14T and Modified 14T Full Adder

Adder Cell	No. of transis-tors	Technol-ogy	Sup-ply volt-age	Bias Volt-age	Avg. Pow er (nW)
14T	14	45nm	0.7V	0.7V	302
Modi-fied 14T	14	45nm	0.7V	0.7V	41.4

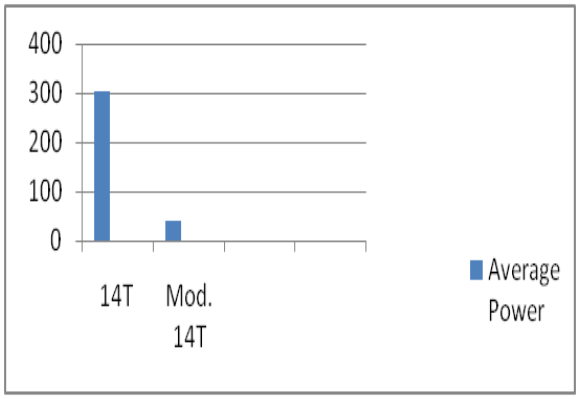

Figure 3 Average Power

Propagation Delay

The propagation delay or average delay times τ_{PHL} an τ_{PLH} determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output,

respectively. By explanation, τ_{PHL} is the delay time between the V50% change of the increasing input voltage and the V50% change of the dropping output voltage. Also, τ_{PLH} is signified as the delay time between the V50% change of the dropping input voltage and the V50% change of the increasing output voltage [11].

$$\tau_p = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

Table 3: Average Delay in 14T and Modified 14T Full Adder

Adder Cell	No. of transis-tor	Tech-nology	Sup-ply volt-age	Bias Volt-age	Avg. Delay (ns)
14T	14	45nm	0.7V	0.7V	8.56
Modified 14T	14	45nm	0.7V	0.7V	8.43

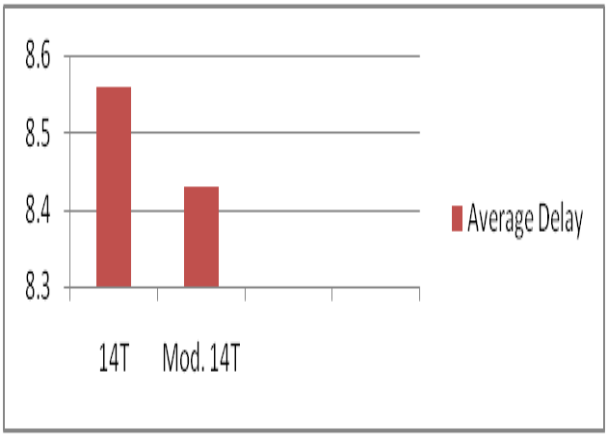

Figure 4: Average Delay

Table 4: Leakage Power in 14T and Modified 14T Full Adder

Adder Cell	No. of transis-tors	Tech-nolog y	Sup-ply volt-age	Bias Volt-age	Leak-age power
14T	14	45nm	0.7V	0.7V	61.43 (10^{-12})
Modified 14T	14	45nm	0.7V	0.7V	74.8 (10^{-14})

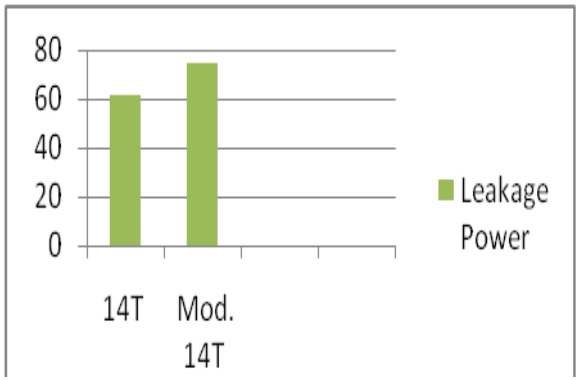

Figure 5: Leakage Power

Following are the waveforms of both full adders the 14t and the modified 14T carried out after the simulations:-

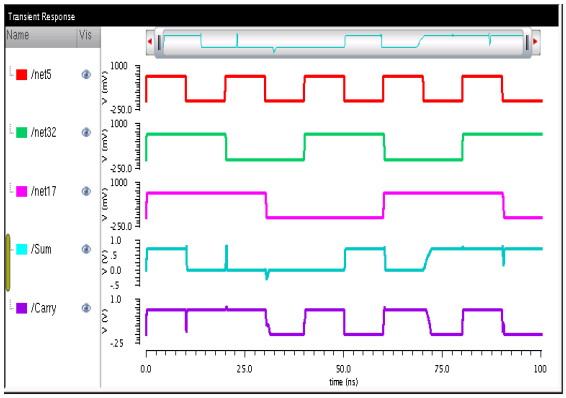

Figure 6: Waveforms of 14T Full Adder

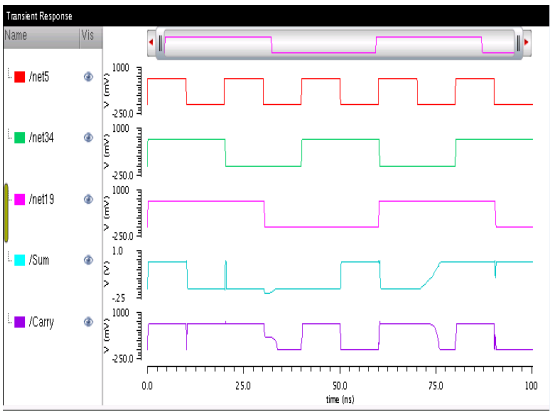

Figure 7: Waveforms of Modified 14T Full Adder

7. CONCLUSION

In the present work conventional 14T full adder is modified and there performances are compared. The Body Biasing method is applied to conventional 14T Full adder to reduce its Leakage power and Power consumption. The motive of employing the technique to the 14T adder is proven to be

efficient in decreasing Leakage power with Power consumption. Both Adders are compared on the basis of Average Power, Average Delay and Leakage power and it can be clearly seen that performance of full adder is enhanced to a great a level by indulging body biasing to it. The Power consumption is reduced, the delay is reduced.

Thus we can conclude that we can enhance the performance of Full adder employing Body biasing technique. As the chip size is size reducing day by day, researchers are finding new ways to reduce the size and increase the performance, such techniques helps researchers to decrease the figure of merit i.e., PDP without going for a all new design. Modifications seems to be a better option.

8. ACKNOWLEDGEMENT

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