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Booth Multiplier Implementation Using Low Power Finfet Technique

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Abstract*—The basic operations used in any circuit are addition and multiplication as all the other operations such as subtraction, filtering and convolution are performed by the help of these operations only. In digital signal processing the main task is to perform the inner product, sampling and convolution which is mainly performed by the help of multiplier only. Hence to overcome a problem of problem of delay and power consumption the use of digital multiplier instead of analog multiplier takes place. This paper introduced a low power booth multiplier. In a booth multiplier the multiplication take place with the help of shifting, addition and partial product. The booth multiplier consists of a three section decoder, partial product generation unit and adder circuit. The booth multiplier recodes the input value to the booth equivalent value to reduce the switching activity in a circuit. This paper consist a booth multiplier design using a power reduction techniques called FINFET and the result is compared with the result of GDI and CMOS. The implementation of a booth multiplier takes place using a cadence virtuoso. The result obtained is compared in term of average power and noise by the help of various reduction techniques in 45nm technique. The input voltage in this paper varies from 0.5 to 0.7 V.*

Keywords:*—Booth multiplier, cadence virtuoso and multipliers.*

1. INTRODUCTION

As the advancement in technology take place in VLSI, many researcher proposed a circuit which offer more number of transistor and IC's in a single chip also the power consumption and noise is reduces. The key component for any system as it used to perform various function such as filtering. Multipliers with a high clock frequency are the heart of any digital signal processing system. Nowadays the main use of digital system processing block is in the personal mobile communication [1]. Hence the many computational problem is occurs or can be solved by the speed of multiplier used in it as it performs a major role like digital filtering, inner product and convolution [2,3]. Digital multiplier is preferred over analogue multiplier due to less area, lowered the memory requirement for transmitting given amount of data, interconnection requirement to implement the circuit is lowered and also the less power consumption. With the increase in demand of battery powered devices the power consumption and noises becomes a very important factor [4]. There are several power reduction techniques present from which CMOS, GDI and PTL is the very important technique used for power reduction. The CMOS technique offers easy implementation of transistor in any circuit it are valid for booth analog and digital design [5]. The GDI technique is used to offer the improved logic swing hence the power consumption is

reduced, but due to problem of low voltage swing it is difficult to implement the GDI logic in analog circuit [6, 7].

2. FINFET INTRODUCTION

FinFET is used to overcome the issue of sweet – faced due to the mosfet. The full form of FINFET is the field effect semiconductors which providean additional property to the mosfet. It has some advantages over the MOSFET technique like short gate channel chattel effect and corner result corner. Due to the FinFET technique the power consumption in system is reduced as compared to the CMOS technique also the delay produced in the system is reduces due to the use of FinFET technique. However this technique is less effective than some of the technique like GDI and PTL technique. In FinFET technique there two types' short gate and open gate in short gate technique gate terminal get shorted to the drain.

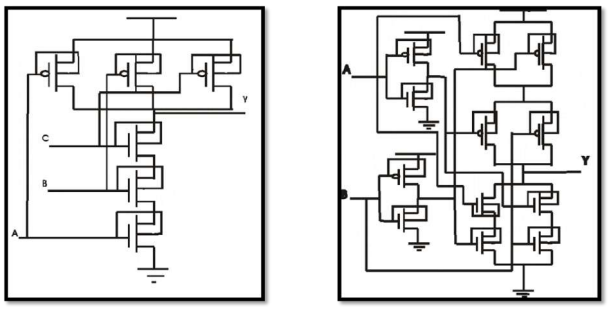

Figure 1. Input NAND gate and XOR gate using a short gate FINFET technique

3. MODIFIED BOOTH MULTIPLIER

The main objective of booth multiplier is to perform a high speed and low power consumption. As the speed and the power consumption of a multiplier is depend upon the partial product so in modified booth multiplier the partial generating unit is reduces to half due to which the delay and power consumption reduces. The maximum delay in a multiplier can be determined by the help of a sum of a delay occur due to the partial product unit. The main task of the booth multiplier is to convert the input bits into the booth equivalent value. There are mainly three sections in booth multiplier those are booth decoder, partial product generating unit and adder circuit.

Booth Decoder

The working of booth decoder is to contained more number of zero's by converting input bits to equivalent bits.

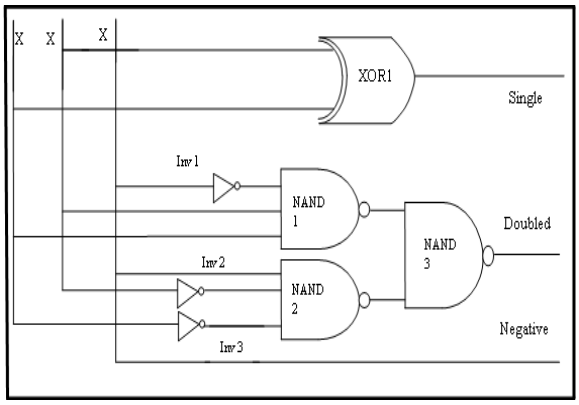

Figure 2. Booth encoder circuit diagram

Partial Generating Unit

The working of partial generating unit is to perform a partial product of output of booth decoder and of the input multiplier bits. The booth product generating unit consist of two basics gates and NAND gate and XOR gates. Then the output of booth partial generating unit is provided to the adder for further shifting operations.

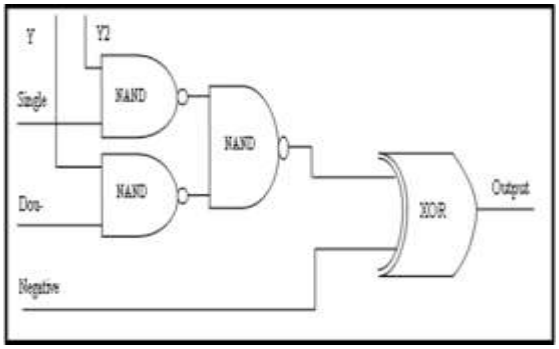

Figure 3: Booth Partial Generating Unit Diagram

4. RESULT AND SIMULATION

The simulation of a booth multiplier using the FINFET technique and CMOS technique and is carried out and compares them. The simulation performed done using software Cadence Virtuoso at 45 nm. The

result obtained in terms of average power and noise. The input value of a voltage taken is 0.7 volt. Here the simulated waveform show that the switching activity in CMOS technique is more as compared to GDI technique and FINFET technique also the power consumption in FINFET is less than CMOS. Result obtained is in the term of average power and noise in a circuit.

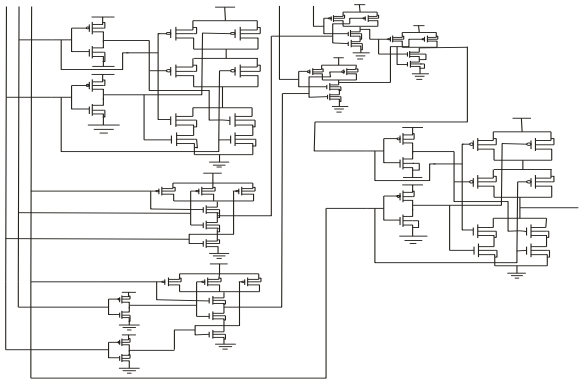

Figure 4. CMOS implementation of booth multiplier

Table 2. CMOS average power and noise

Input Value	Average Power	Noise
0.5 V	43.89 e^{-9}	3.886 e^{-16}
0.6 V	43.98 e^{-9}	3.898 e^{-16}
0.7 V	49.53 e^{-9}	3.899 e^{-16}

The above table shows the average power and noise of the booth multiplier using CMOS technique. Here with the help of table is it clear that the average power and noise of the multiplier is increase on increasing the input power of the multiplier.

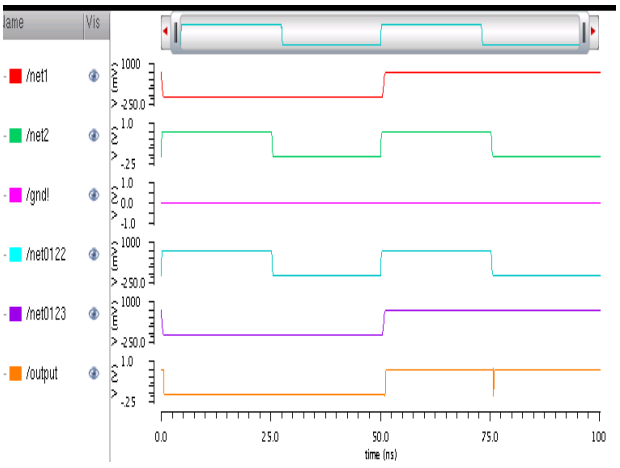

Figure 5. Waveform of CMOS implemented booth multiplier

The above figure represents the input and output of the booth multiplier.

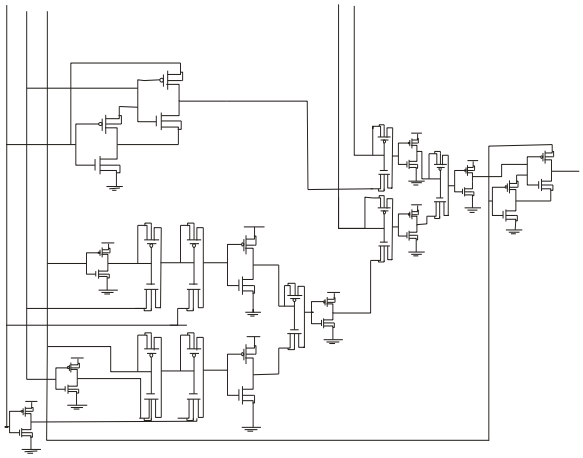

Figure 6. GDI implementation of booth multiplier

The above given figure represent the implementation of booth multiplier using GDI techniques. From the above figure it is clear that transistor used in GDI techniques is less then transistor used in CMOS technique which help in reducing the average power and noise of the booth multiplier.

Table 4. GDI average power and noise

Input Value	Average Power	Noise
0.5 V	18.34 e^{-9}	4.378 e^{-12}
0.6 V	21.13 e^{-9}	4.379 e^{-12}
0.7 V	23.74 e^{-9}	4.379 e^{-12}

From the above table it is shown that the in GDI technique also with increase in voltage supply the noise and average power consumption of the circuit is also increases.

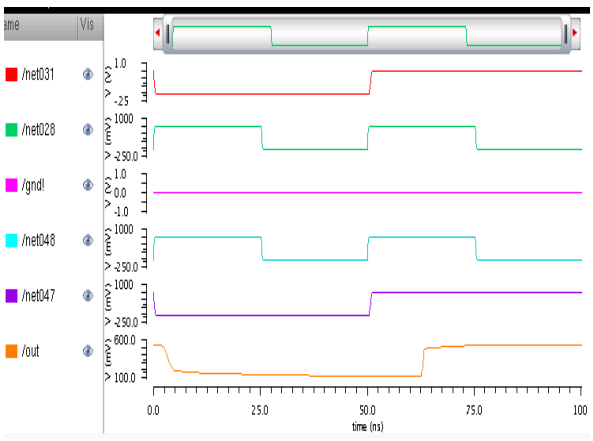

Figure 7. Waveform of GDI implemented booth multiplier

From the above waveform of GDI technique it is clear that the linearity of the circuit is also improves because the output of the multiplier not suddenly changes with the change in input techniques.

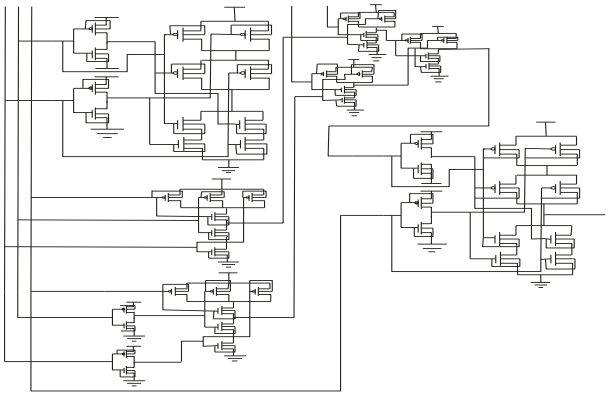

Figure 8. FINFET implementation of booth multiplier

The above figure shows a transistor level diagram of the booth multiplier using short gate FinFET technique short gate technique is basic FinFET technique. In this technique the gate terminal is connected to the body terminal of the transistor.

Table 3. FINFET Average Power and Noise

Input Value	Average Power	Noise
0.5 V	35.256 e^{-9}	5.817 e^{-15}
0.6 V	36.278e^{-9}	5.807 e^{-15}
0.7 V	38.574 e^{-9}	5.837 e^{-15}

The above table represent the average power and noise of the booth circuit at different input power which varies from 0.5 V to 0.7 V.

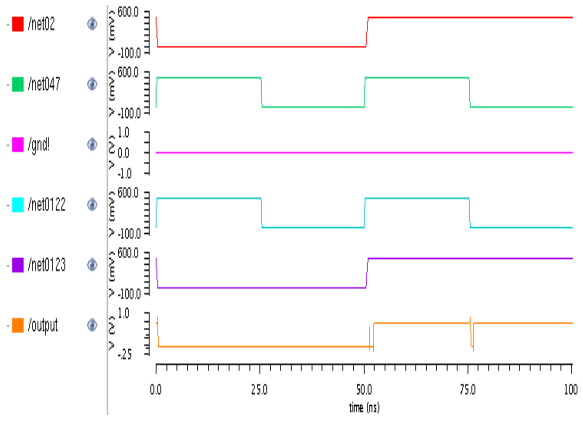

Figure 9. Waveform of FINFET implemented booth multiplier

The above table and the waveform represent the implementation of the booth multiplier suing FinFET technique.

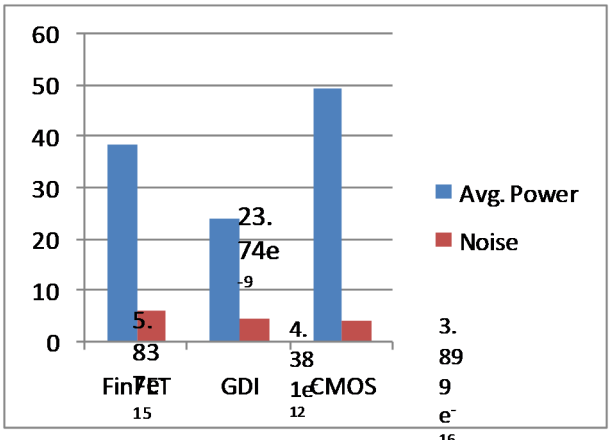

Figure 10. Comparison graph between FinFET, GDI and CMOS technique.

From the above comparison graph it is clear that the GDI technique is better than the FinFET technique and CMOS techniques in terms of power consumption and noise due to the improved linearity of the circuit and the less use of transistor.

5. CONCLUSION

In this paper a modified booth multiplier implemented using FINFET, CMOS and GDI technique in 45 nm using a tool cadence virtuoso and compared with the result of CMOS technique. With the help of output value we conclude that the FINFET technique is better than the CMOS technique but less good than GDI technique in terms of power consumption and noise, as it reduces the switching of output value with the sudden change in inputs value also the area reduce with the reduction in transistor used in a circuit.

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