ISSN 2320-9984
Volume 5 Issue 1 | March 2017 ISSN: 2320-9984 (Online)
International Journal of Modern Engineering & Management Research
Website: www.ijmemr.org

Speed Efficient Fast Carry Select Adder Using Modified BEC

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Abstract**—***To perform the fast arithmetic functions in many data processing processors at low cost, carry select adder is the most suitable adder among the various adders To design the power and area proficient fast speed data path logic systems, the field of very large scale integration (VLSI) is the generally significant area of research where minimize the area and power is the more difficult task. In digital system, mostly adders lie in the crucial paths that affect the whole performance of the system. Experimental analysis illustrates that the proposed architecture achieves advantages in terms of speed, area consumption and power.*

Keywords:— *Carry Select Adder, adder, mux, VLSI, BEC*

1. INTRODUCTION

Outline of area and power effective rapid information rationale frameworks are a standout amongst the most considerable areas of exploration in VLSI framework plan. In gadgets applications adders are most generally utilized. In computerized adders, the speed of expansion is restricted when needed to engender a carry through the snake. The aggregate for every bit position in a elementary adder is produced consecutively strictly when the past bit position are summed and carry spread into the following position [1].

The CSLA is utilized as a part of numerous computational frameworks to allay the issue of carry spread postpone by free era different conveys and afterward select a carry to create the aggregate. On the other hand, the CSLA is not an area productive on the grounds that it utilizes different sets of Ripple Carry Adders (RCA) to produce halfway total and carry by considering carry include as C_{in}=0 and C_{in}=1, then the last summation and carry are chosen by the multiplexers. The Carry select adders are delegated Linear Carry select adders and Square-root carry select adders [2]. The fundamental square-root Carry Select adders has a double ripple carry adder with 2:1 multiplexer, the principle detriment of consistent CSLA is the expansive area because of the different sets of ripple carry adder.

In this paper, modified CSLA using BEC has introduced to reduce area and power consumption with slight increase in delay. The basic idea of the proposed architecture is that which replaces the BEC by common Boolean logic with enable signal[9]. The proposed architecture reduces the area, delay and power [10]. This paper is organized as follows; section 2 review the related works and section 3 presents the detailed structure of proposed methodology. Results are analyzed in the section 4. Section 5 concludes the paper[11].

2. LITERATURE SURVEY

The author introduced a carry select adder (CSL) to reduce the delay as compared with the other existing adders. This adder has a deepness of knowledge in logarithmic gate to

design any of the formation an adder's family. The ripple-carry adder (RCA) is used in CSL which leads to less performance. So one of the fastest adder called Carry Select Adder (CSLA) is used to carry out the arithmetic operation as earlier. The CSLA is a best adder that provides optimal result in VHDL execution and it may effectively diminish the CSLA parameters. The simulation result shows that the modification 32-b CSLA (CSLA) structural design gives better result as compared with the other techniques is studied in [3].

In [4] a hybrid full adder with low power multipliers is used. In [5] the Ripple carry adder shows the evidence of unsophisticated designs of the circuit but it speed is slow. The carry look ahead adder (CLA) is one of the best one but it occupies large area. CSA is act as a concession between two adders like Ripple carry adder and carry look ahead. 32-Bit Multiplier with a CLA and a 32-bit Multiplier with a RCA are implemented in VHDL to analyze the performance is studied in [6]. In [7] the author presents a square-root CSLA (SQRT CSLA) which reduces the area and the power as it is compared with the other techniques to evaluate the performance.In [8] proposed a BEC method to minimize the carry propagation delay in final stage of carry save adder.

3. PROPOSED METHODOLOGY

A Carry Select Adder is a particular way to implement an adder, which is a logic element that computes the (n+1) bit sum of two n-bit numbers. The carry-select adder is simple but rather fast. The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. By sharing the common Boolean logic term in summation generation, a proposed carry select adder design is illustrated in Fig 1[12]. To share the common Boolean logic term, it only needs to implement one OR gate with one INV gate to generate the Carry signal and summation signal pair. Once the carry-in signal is ready, then select the correct carry-out output according to the carry-in signal logic state[13]. As compared with the Modified Carry Select adder, the proposed CSLA is little bit faster, but the speed is nearly equal to the Regular CSLA. The delay time in our proposed adder design is also proportional to the bit number N; however, the delay time of multiplexer is shorter than that of full adder. The Proposed CSLA is Area efficient & low power, but the speed equal to the Regular CSLA.

Table 1. The truth table of single bit FA and single-bit full-adder with Modified BEC

C_{in}	A	B	S_0	C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

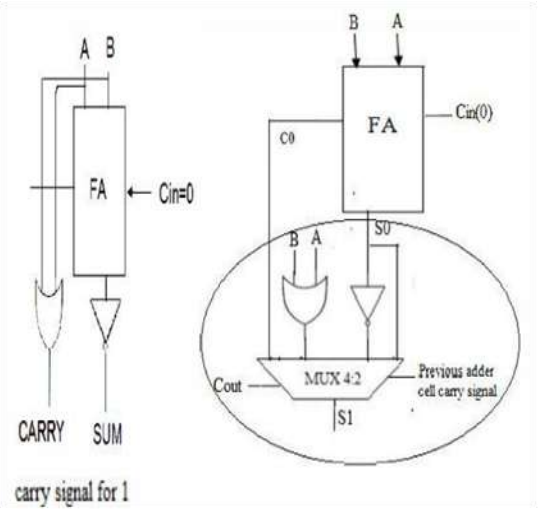

Figure 1: Single bit FA with Modified BEC

3.1 Modified CSLA Architecture

This method replaces the BEC add one circuit by Common Boolean Logic. The output of full adder waveform for carry in signal is 'I ' and it generates the carry signal and summation by just using an OR gate and INV [18]. It is shown in figure 2.

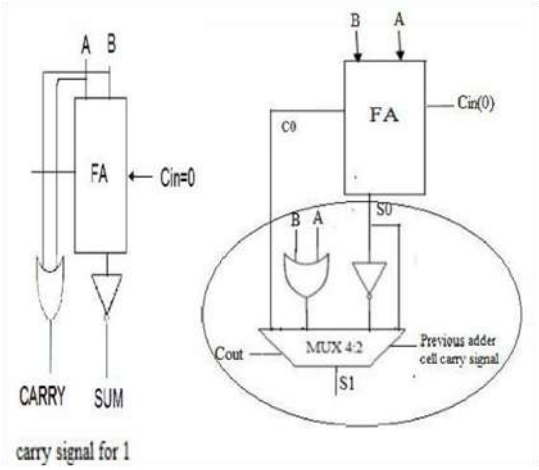

Figure 2: 16-bit SQRT CSLA using Modified BEC

The carry signal and summation for FA which has Cin=l, it is generated by the INV and OR gate. With the help of multiplexer, we can predict the correct output result according to the logic state of each carry-in signal. Internal structure of the group 3 of Proposed CSLA is shown Fig 3. A Manual counting of number of gates is used for group 3 is equal to 36 (full adder, half adder, and multiplexer, not, or gate)[12]. One input to the mux goes from the RCA block with Cin=O and other input from the CBL.

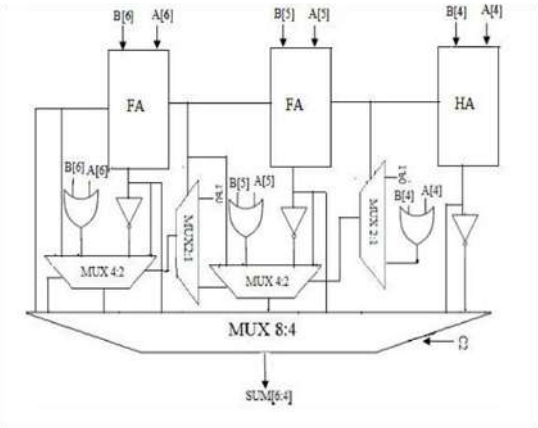

Figure 3: Modified BEC

The Group 3 performed a three bit addition which are A [4] with B [4] , A[S] with B[S] and A[6] with B[6]. This is done by I half adder (RA) and two full adder (FA). The CBL block has a 4:2 multiplexer to select the appropriate carryout and summation signal for Carry-in signal ' I '. Through 2: I multiplexer the carry signal is propagate to the next adder cell. The 6:3 multiplexer and 4:2 multiplexer is the combination of 2: I multiplexer[14].

4. PERFORMANCE EVALUATION

The proposed design used in this research work has been developed using synthesized in Cadence RTL compiler using typical libraries of TSMC 0.18 um technology Verilog- HDL. The synthesized Verilog netlist and their respective design constraints file (SDC) are imported to Cadence SoC Encounter and are used to generate automated layout from standard cells and placement and routing. Parasitic extraction is performed using Encounter's Native RC extraction tool and the extracted parasitic RC (SPEF format) is back annotated to Common Timing Engine in Encounter platform for static timing analysis. The performance of the proposed approach is evaluated using the performance metrics such as Delay, area and power. Several real time implementation strategies were discussed in [15],[16] and [17].

4.1 Timing Analysis

The Timing analysis has been done in ISE simulator the output obtained is shown in figure 6.

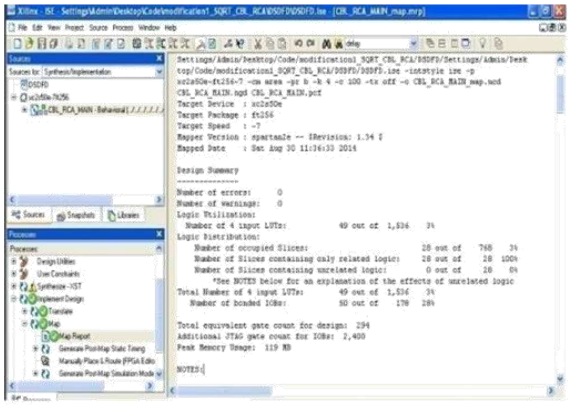

Figure 4: Timing Analysis

4.2 Comparison

In the following given table which target FPGA has been used belongs to Spartan 3 (family), XC3S400 (device), TQ144 (Package), -5 (speed grade).

Table 2. Comparison Table

Maximum Combinational Path Delay (in ns) for different Carry select adder at 16 bit level		
M.N.V. Anusha, K. Babulu[5]	S. Balaprasad [3]	Result Obtained
17.21	27.1	15.138

5. CONCLUSION

In this paper analyzed the logic operations involved in the conventional and BEC-based CSLAs to study the data dependence and to identify redundant logic operations. And also eliminated all the redundant logic operations of the conventional CSLA and proposed a new logic formulation for the CSLA. The modified SQRT CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-I converter. This paper proposes a scheme which reduces the delay, area consumption and power than regular and modified CSLA by the use of modified BEC. In future work, It would be interesting to test the design of the proposed 128-b SQRT CSLA by Quantum dot Cellular Automata (QCA) method. In brief, we propose another adder, that achieves all conditions of competitors and accomplishes the best area-delay tradeoff by using a majority gate. The above preferences are obtained by utilizing an overall area/space to the less expensive plans as known in the literature.

REFERENCES:

[1] Varsha Viswam, Suchithra S Nair, "VHDL Architecture for Delay Efficient SQRT Carry Select adder", IJARCSSE ,Volume 6, Issue 6, June 2016.

[2] Anitha. K, Mangala Mari Selvi, "Analysis of Carry Select Adder Using Zero Carry Look Ahead Adder" IJIRCCE, Vol. 4, Issue 3, March 2016

[3] S. Balaprasad, M. Jeyalakshmi," Area Efficient Carry Select Adder with Low Power", IJEEE, Volume 2 Issue 2 Feb 2015.

[4] Sanooja S, Aswathi B, "A Modified Carry Select Adder Using Common Boolean Logic", IJETR ISSN: 2321-0869 (O) 2454-4698 (P), Volume-3, Issue-7, July 2015.

[5] M.N.V. Anusha, K. Babulu , "Design and Analysis of Carry Select Adder with RCA and BEC Circuits", IJSETR, Volume 3, Issue 11, November 2014.

[6] D. Kumaresan1, D. Jeyamani M.E, "A Modified BEC Logic Design of High Speed CSLA for Low Power And Area Efficient Applications", ICGICT,Vol.2, Special Issue 1, March 2014.

[7] Basant Kumar Mohanty and Sujit Kumar Patel "Area–Delay–Power Efficient Carry-Select Adder", IEEE Transactions On Circuits and Systems—II: Express Briefs, Vol. 61, No. 6, June 2014.

[8] Pinnika Venkateswarlu, Ragutla Kalpana, "An Efficient SQRT Architecture of Carry Select Adder Design by HA and Common Boolean Logic", IJECE, Volume 1 Issue 8 Oct 2014.

[9] Veena V Nair, "Modified Low-Power and Area-Efficient Carry Select Adder using D-Latch", IJESIT, Volume 2, Issue 4, July 2013.

[10] Ishita Banerjee, "High Speed, Low Power, Area Efficient Mux-Add and BEC Based Implementation of Carry Select Adder", IJREA ISSN: 2248-9622, Vol. 3, Issue 6, Nov-Dec 2013.