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Power Efficient Design of 4:1 Multiplexer using Low Power Techniques

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Abstract**—***Low power, high speed and area efficient design for digital gadgets are fundamental requirements of digital circuits that used in VLSI. Multiplexer is a primary cell for every digital circuit. In this paper, I design and simulate 4*1 multiplexer using conventional and NMOS, TGL, DPTL techniques. I have also done comparatively study with conventional CMOS Design on the principle of transistor count, speed, power dissipation and area. TGL is formed by parallel NMOS and PMOS transistors. It is capable of passing both '1' and '0' and reduces circuit complexity and removes degraded output. A basic DPTL structure consists of PMOS and NMOS transistors connected in parallel and it generates dual logic function. Using NMOS base multiplexer is a finest logic design which has quality of high speed with least power and reduces number of transistor count. Cadence tool is used for simulation of results on 45nm technology.*

Keywords**:—***CMOS, TGL, NMOS, DPTL, power dissipation, speed, transistor count.*

1. INTRODUCTION

Modern era of transportable devices such as cell phones, laptops power dissipation has turn out to be main concern in VLSI design. Because batteries supplied partial power, the circuits are designed to consume least power and dimension of electronics devices are getting reduced day by day. As a result, size of battery reduces in same fraction building device lighter [1]**.** Battery efficiency can be improved either by making the size of the battery greater, but it makes the device bulkier or by designing the circuit which consumes less power. The CMOS circuit consume very less power consumption, but a major power issue of the CMOS circuit is the dynamic power. In the CMOS circuit, for the duration of voltage supply, during transition 0 to v_{dd} , c v_{dd}^2 energy has been drawn up from the DC power supply. Pull-Up network consumed half of the energy and $\frac{1}{2}$ c v_{dd}^2 only energy stored at the output load. During the power supply transition from v_{dd} to 0, the stored energy at the output load gets dissipated to ground through pull down network. So in the CMOS circuit, the total power dissipation is c v_{dd}^2 for one cycle of operation [2].

Multiplexer's square measure is a typical structure cell for data-paths, and is used widely in a variety of applications together with the processors [3]. The electronic device circuit is usually used to mix two or additional digital signals into single line. Theoretically, Mux can be called as time-division multiplexing. They are also used in programmable logic devices [4]. Multiplexer is a fundamental component in digital design. A

multiplexer is a circuit which selects one of 2^n input signals and passes the selected input to output. Switch logic is used in multiplexers. Switch logic is the logic in which circuits are realized as arrangement of switches, not from logic gates. With the help of Multiplexers we can easily design CPUs and graphics controller and programmable logic devices, in computer networks and digital video [5].

Combinational circuits are implemented by multiplexers. So by using finest circuit of multiplexers, we can easily simplify any circuit which is made up of combinational circuit [6].

2. MULTIPLEXER4:1

Multiplexer is a circuit in which n select lines select one of 2^n input lines and selected line goes to output. Multiplexer is a fundamental component in designing control systems and dynamic circuits [7]. To increase the quantity of data which is sent through system within a definite duration of time and bandwidth multiplexers are used. A Multiplexer can be called as data selector [8].

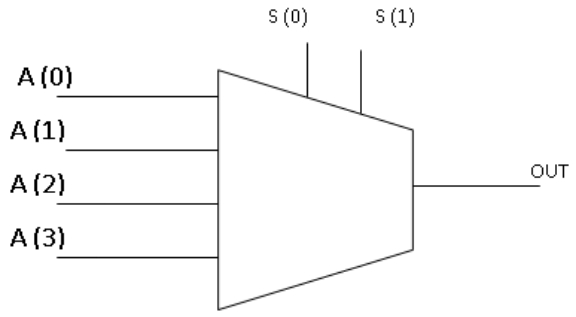

Figure 1: Conventional 4:1 multiplexer

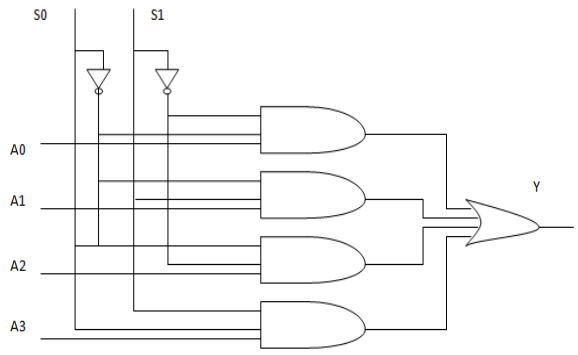

Figure 2: (a) Gate Implementation of 4:1 Multiplexer

Multiplexer has two select lines S(0) and S(1) which are used for selection and four sets of inputs A(0),A(1), A (2), A(3). The Multiplexer output is in a single bit Y, which is one of the 2^n input data.

S(1)	S(0)	Y
0	0	A(0)
0	1	A(1)
1	0	A(2)
1	1	A(3)

Figure 2: (b) Truth Table of 4:1 Mux

3. Different Logic Styles: Logic style can be defined as how transistors are used to realize logic function. Speed, size, power dissipation and wiring complication are the features which rely on which logic style is used and they are vary noticeably from one logic style to other logic styles and therefore, for circuit concert selection of appropriate logic style is very helpful. Complementary MOS and NMOS, TGL, DPTL four techniques are used in this paper.

3.1 Complementary MOS Logic Style

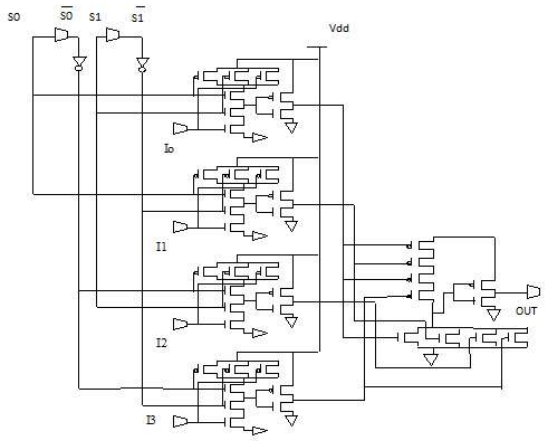

Figure 3: Conventional CMOS base 4:1 Multiplexer

Both N-type and P-type transistors are used in Cmos logic style to design logic functions. Both p-type and n-type transistors are joined to the identical input, one type of MOSFET will be immediately on when other MOSFET is off, and vice-versa. In CMOS logic gates n-type MOSFETs are sand witched

between the lower voltage power supply rail and output and it is used in a pull down network and p-type MOSFETs are used in a pull up network sand witched between the higher voltage rail and the output. Problem of voltage scaling and transistor sizing is not more in CMOS circuits [9]-[10].

3.2 Transmission Gate logic (TGL)

X	IN	OUT
H	H	H
H	L	L
L	X(don't care)	Z(high impedance)

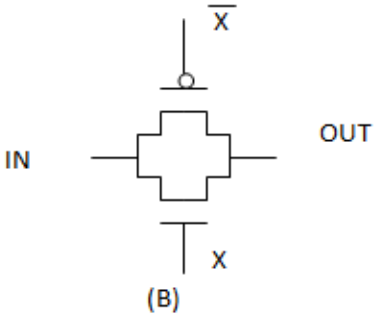

Figure 4: (a) Truth Table (b) Transmission gate

4:1 mux using Transmission gate type is formed when PMOS is connected in front of NMOS and it works as a switch. NMOS devices pass a strong zero but a weak 1, while PMOS pass a strong one on the other hand, a weak 0[11]. In TGL neither transistor is connected to VDD or GND. The transmission gate takes the finest properties from both type of transistor by inserting NMOS in front of PMOS device. Four transmission gates square measure are used to create an MUX structure [12].

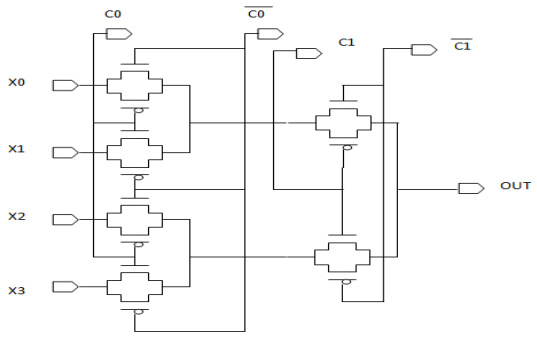

Figure 5: TGL base 4:1 Multiplexer

3.3 DPTL (Dual Pass Transistor Logic)

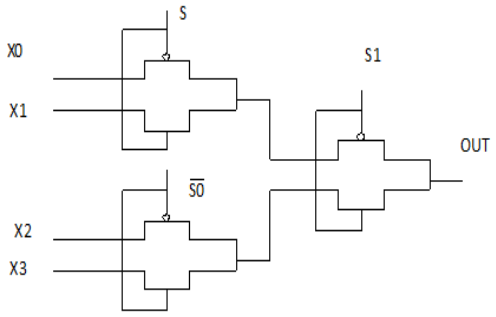

Figure 6: DPTL base 4:1 Multiplexer

The powerful formation in CMOS technology is Dual Pass Transistor Logic (DPTL). In spite of input signal-swing deviation, DPTL buffers have the capability to create standard CMOS levels. A basic DPTL structure consists of PMOS and NMOS transistors connected in parallel [12]. Dual logic function in DPTL is generated by exchanging NMOS and PMOS, VDD and GND.

3.4 NMOS logic

In NMOS logic six NMOS transistors are used to design 4:1 multiplexer and at the input these pass transistors are used to select which signal is transmit. The threshold voltage of both pass-transistors of single unit of 2:1 multiplexer should be Identical for precise operation. It reduces transistor count and takes less power [13].

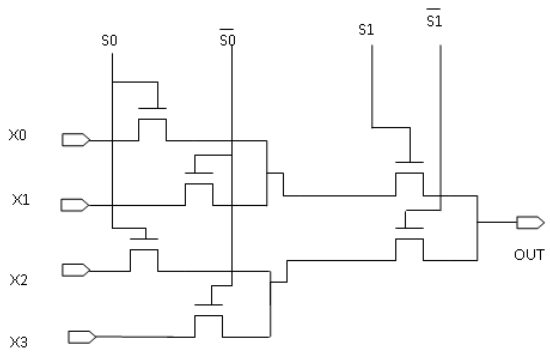

Figure 7: NMOS base 4:1 Multiplexer

4. SIMULATION RESULTS

In this section, output waveforms of Cmos, Transmission gate logic, Dual pass

transistor logic and NMOS logic are showed and results of these circuits are also calculated.

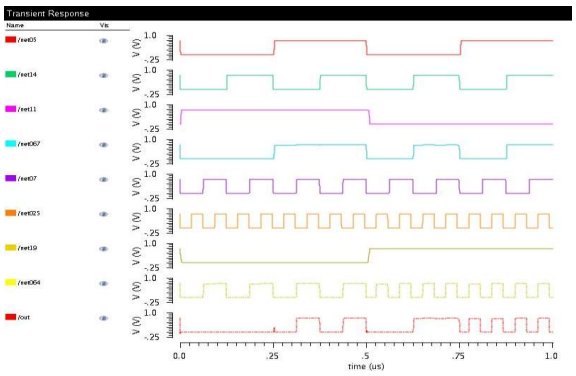

Figure 8: Cmos Waveform

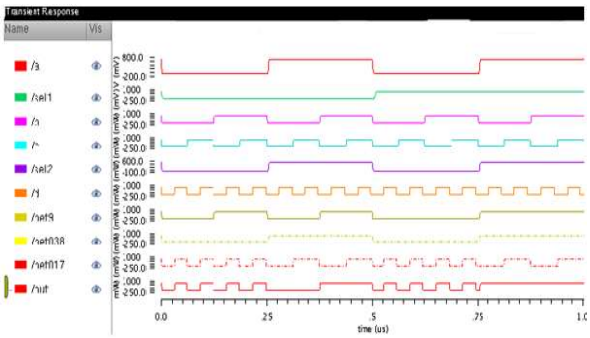

Figure 9: TGL Waveform

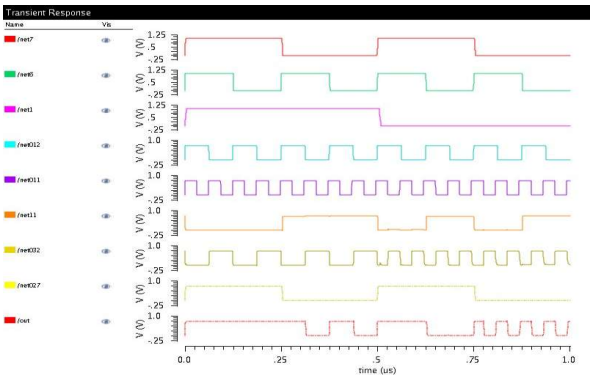

Figure 10: DPTL Waveform

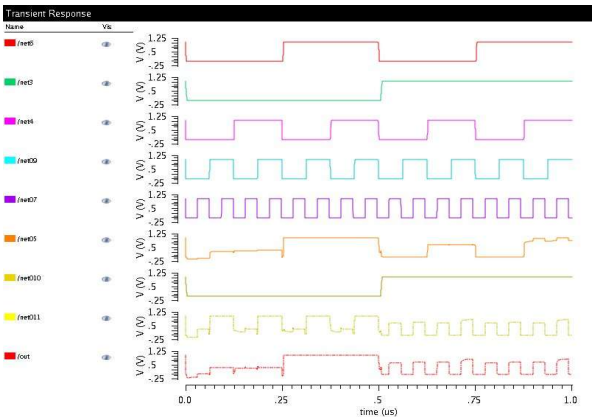

Figure 11: NMOS Waveform

These figures shows that output waveforms of 4:1mux using various techniques. Like Cmos, Transmission Gate Logic, dual pass transistor logic and NMOS techniques. Four inputs are selected by two select lines and one input goes to output. Three 2:1 multiplexer are used to realize 4:1 multiplexer.

4.1 Power dissipation

Power dissipation mechanism is classified into two classes:

A. Static power dissipation and Dynamic power dissipation

- When circuit is in active state Dynamic power dissipation occurs, i.e. some work perform on data.
- due to load capacitances charging and discharging
- When both PMOS and NMOS are moderately on

B. Static power dissipation occurs when the circuit is in off state or in a power -down mode.

- Sub threshold transmission through down mode transistors.
- Tunnelling current passes gate oxide
- Leakage current in reverse-biased diodes

Ptotal= Pstatic + Pdynamic …… (1)

Pdynamic=1/2 (CL*VDD2 *fc)……..(2)

Pstatic = Ioff* VDD……..…….(3)

Where,

CL= load capacitance

VDD=Power supply

fc= Clock frequency

Ioff =leakage current drawn by each switch in off state

4.2 Speed

Speed of digital circuits can be found by: Delay

td= (CL * VDD) /Ion……..(4)

Maximum clock frequency:

fc, max= 1/ (td * Ld)……. (5)

Where, CL= load capacitance

VDD=Power supply

Ion= leakage current drawn by each switch in on state

Ld= logic depth (no of stages through which a switching event must propagate during one clock cycle)

4.3 Transistor Count

The quantity of transistors in the device is called the transistor count. Transistor count is the well-known measure of integrated circuit size.

5. COMPRESSION RESULTS

Technique used	Transis-tor count	Power consump-tion	Delay
conventional	36	75.596uW	0.588ns
DPTL	6	2.544nW	0.053ns
TGL	18	12.887nW	0.075ns
NMOS	6	34.544nW	0.0483ns

6. CONCLUSION

In this paper, the digital circuit 4:1 mux was implemented by different low power techniques namely CMOS, TGL, NMOS, and DPTL. Using cadence results were simulated and comparison has been done for different parameters like power dissipation, delay and transistor count. The results concluded that as compared to other proposed techniques, CMOS has more power dissipation and transistor count. These advantages of proposed techniques over CMOS make them more efficient and convenient to be used in digital circuits.

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