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Analysis and Design of Two-Stage Operational Transconductance Amplifier

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***Abstract*—*This paper presents design concept of Operational Transconductance Amplifier (OTA). The 0.18µm CMOS process is used for Design and Simulation of this OTA. This OTA having a bias voltage 1.8 with supply voltage, the design and Simulation of this OTA is done using CADENCE Specters environment with UMC 0.18µm technology file. The Simulation results of this OTA shows that the open loop gain of about 71 dB which having GBW of 37 KHz also this OTA is having CMRR of 90 dB and PSRR of 85 dB. This paper presents the design and analysis two-stage operational transconductance amplifier (OTA) for use in switched-capacitor (SC) circuits. The existing design methods for two-stage OTAs often lead to sub optimal solutions because they decouple inter-related metrics like noise and settling performance. In our approach, the cadence tool is used to analysis the transient response, AC response and phase plot of the OTA and settling time has been observed on the simulation. For the optimization routine, there is no need to interface with a circuit simulator because all significant devices parasitic are included in the tool.*

***Keywords:*—*Two stage OTA, transient response, power, cadence tool.*

1. INTROUDUCTION

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Hence it is a voltage control current source (VCCS). There is usually an additional input for a current to control the amplifier's therefore, the OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback. Due to recent development in VLSI technology the size of CMOS decreases and power supply also reduces. Thus the OTA is a basic building block in most of analog circuit with linear input-output characteristics also OTA is widely used in analog circuit include such as neural networks and Instrumentation amplifier with ADC and Filter circuit. The operational Transconductance Amplifier (OTA) is basically similar to that of conventional operational Amplifiers in which both having Differential inputs also the basic difference between OTA and conventional operational Amplifier is that in OTA the output is in form of current but in conventional Op-Amps output is in form of Voltage. The OTA is popular for implementing voltage controlled oscillators (VCO) and filters (VCF) for analog music synthesizers, neural networks and instrumentation amplifier because it can act as a two-quadrant multiplier. Fast, high gain operational-transconductance amplifiers (OTAs) are an integral part of switched capacitor (SC) circuits. The primary application for an OTA is however to drive low-impedance sinks such as coaxial cable

with low distortion at high bandwidth. The OTA has been traditionally implemented using a cascade of two stages to provide a high gain. Scaling dimensions in CMOS technology requires proportional scaling in supply voltage as well. Also Through lower supply voltages result in lower power consumption, as the supply currents. Improving the settling performance by Phase-margin adjustments has been proposed in the literature. However, for two-stage amplifiers, better phase margin does not always imply faster settling. An OTA is a voltage controlled current source and also more specifically the term operational comes from the fact that it takes the difference of two voltages as the input for the current conversion.

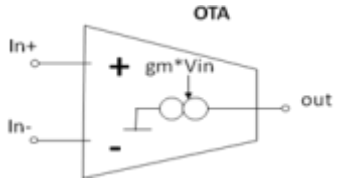

Figure1: Ideal OTA

The ideal for the Transfer characteristics is therefore written as follows by,

$$I_{out} = g_m (V_{in}+ - V_{in}-) \quad (1)$$

Or, by taking the pre-computed difference as the input,

$$I_{out} = g_m * V_{in} \quad (2)$$

With the ideally constant transconductance g_m as the proportionality factors between them two. In reality the transconductance1 is also a function of the input differential voltage and dependent on temperature. To summarize, an ideal OTA has two voltage inputs with infinite impedance (i.e. there is no input current). The common mode input range which is also is at infinite while with the differential signal between these two inputs is used to control an ideal current source (i.e. the output current does not depend on the output voltage) that functions as output and the proportionality factor between the output current and input differential voltage is called transconductance.

2. ANALOG DESIGN AND OPTIMIZATION

For large circuits symbolic analyzers and, or simulators can be used to perform the automated design and optimization.

The gradients and Hessian matrices can be found by two methods. The optimization algorithm can perturb each variable and use the simulator to evaluate the objective and constraints and then compute the gradients and Hessians using finite differences (a slow process), or simply use the symbolic model to find the gradients directly by differentiation over the closed form expressions of the objective and constraints (a fast process).

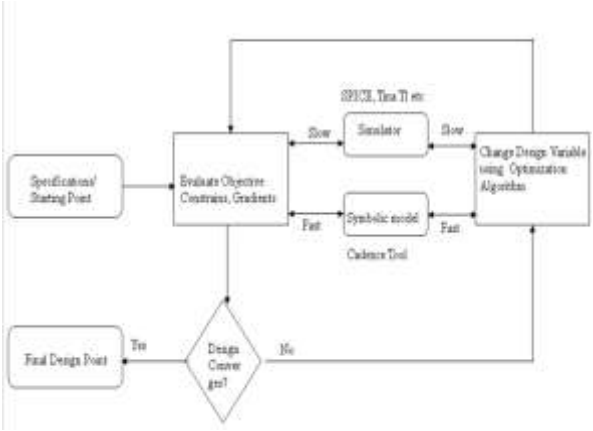

Figure 2: Analog design automation and optimization

Sometimes, the optimizer can reach a design point that is feasible, but finite differences at the lead to an infeasible point which causes the optimizer to diverge or halt prematurely. In such cases, providing gradients and Hessians directly from closed form expressions allows the optimizer to converge to a solution. A typical design optimization loop is shown in Figure 2. The design starts with a certain set of specifications and a beginning point. Thus the performance metrics are evaluated at the current design point. This can be done by going back to the simulator, which is a very slow process. By using a complete symbolic model in cadence tool,

which is faster than the previous, the optimization algorithm then changes the design point to make sure that the objective converges to the optimum and the constraints are met.

We thus conclude that finding the gradient using finite differences can be time consuming, can lead to inaccurate results, and may even cause the optimizer to fail. This can be especially problematic when the optimizer needs to be run multiple times with new beginning point in order to find the globally optimal design point. Each optimizer run itself involves multiple transient, noise, and ac simulations. This leads to impractically long run times if a circuit simulator is used, even for small and medium sized circuits. All these problems can be overcome if closed form symbolic expressions are available and are used for generating the gradients and Hessians. Such Expressions speed up computer-based optimizations, and can sometimes provide designers with design in-sights and trade-offs, letting them make intelligent design choices. Designers can use closed form equations to analyze a circuit and prepare a fixed design plan that can be used for the knowledge-based approach to analog design automation.

3. TWO-STAGE OTA DESIGN AND OPTIMIZATION MODEL DESCRIPTION

In this section, we describe the model used for the design and optimization two-stage OTA using cadence tool. The CMOS level implementation of the OTA is shown in Figure 3.

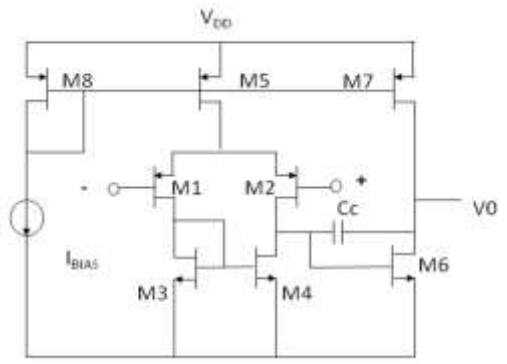

Figure 3: Two stage CMOS operational Amplifier

3.1 Input Resistance, Output Resistance and Open-circuit Voltage Gain

The first stage in Figure 1 consists of a p -channel differential pair M1-M2 with an n-channel current mirror load M3-M4 and a p-channel tail current source M5. The second stage consists of an n-channel common-source amplifier M6 with a p-channel current-source load M7. Because the OP-AMP inputs are connected to the gates of MOS transistor, the input resistance is essentially infinite when the OP-AMP is used in internal applications. For the same reason, the input resistance of the second stage of the OP-AMP is also essentially infinite. The output resistance is the resistance looking back into the second stage with the OP -AMP inputs connected to small signal ground.

$$R0 = r\ 06 \parallel r\ 07$$

Where R0=output resistance and ro6 and ro7 are the internal resistance of transistor M6 and M7 respectively. Although this output resistance is almost always much larger than in general purpose bipolar OP-AMP, low output resistance is usually not required when driving purely capacitive loads. Since the input resistance of the second stage is essentially infinite, the voltage gain of the amplifier in Figure 1 can be found by considering the two stages separately. The small signal voltage gain of first stage (basic diff amp) is given by

$$A_{V1}\frac{V01}{Vi} = G_{m1}R_{01}$$

Where $A_{V1,}$ gm1, and Ro1 are output voltage of first stage, input differential voltage, the transconductance and output resistance of the first stage respectively

$$Av1 = gm1(r\ 02 \parallel R04)$$

Where Av1, gm1, ro2, R04 are the voltage gain of first stage, transconductance of transistor M1, internal resistance of M2 and output resistance of M4 respectively, similarly the second stage voltage gain is

$$Av2 = gm6R0$$

Where R0 is given in (2.1).As a result, the overall gain of the amplifier is

$$Av = Av1Av2 = gm1(r\ 02 \parallel r\ 04)\ gm6\ (r\ 06 \parallel ro7) \quad (5)$$

This equation shows that the overall gain is related to the quantity $(gmr0)^2$

$$\mathbf{gmr_0 = \frac{2v_A}{V0_V}}$$

Therefore, the overall voltage gain is a strong function of the early voltage and the overdrive. In which early voltage (VA) is proportional to the effective channel length and V_{0V} is set by the bias conditions. The overall gain can be increased by either increasing the channel length of the devices to increase the early voltages or by reducing the bias current to reduce the overdrives.

3.2 Output Swing

The output swing is defined to be the range of output voltage V0=V0+v0 for which all transistors operate in the active region so that the gain calculation in (5) is approximately constant. From inspection of Figure 1, M6 operates in the triode region if the output voltage is less than Vov6-Vss. Similarly, M7 operates in the triode region if the output voltage is more than VDD-|Vov7|.Therefore, and the output swing is

$$Vov6\text{-}Vss \leq Vo \leq VDD\text{-}|Vov7|$$

Where V0v6 and V0v7 show the overdrives voltage of M6 and M7 respectively, this inequality shows that the OP-AMP can provide high gain while its output voltage swings within one overdrive of each supply. Beyond these limits, one of the output transistors enters the triode region, where the overall gain of the amplifier would be greatly diminished. As a result, the output swing can be increased by reducing the overdrives of the output transistors.

3.3 Input Offset Voltage

The input offset voltage of a differential amplifier was defined as the differential input voltage for which the differential output voltage is zero. Because of the OP-AMP in Figure 1 has a single-ended output, this definition must be modified here. The voltage between the output node and ground as the output voltage, the most straightforward modification is to define the input offset voltage of the OP-AMP as the differential input voltage for which the OP-AMP output voltage is zero. This definition is reasonable if VDD=VSS because setting the output voltage to zero maximize the allowed variation in the output voltage before one transistor operates in the triode region provided that Vov6=|Vov7|.

4. SIMULATION

In this paper the design of this operational transconductance amplifier (OTA) is done using Cadence Tool. The Simulation results are done using Cadence Spectre environment using UMC 0.18 µm CMOS technology. The simulation result of the OTA shows that the open loop gains of approximately 71 dB. The OTA has GBW of about 37 KHz. The Table 1 shows that the simulated results of the OTA. The AC response which shows gain and phase change with frequency.

Table1. Simulated characteristics of OTA

Specifications	Simulated
CMOS Technology	0.18µm
Open loop gain	71dB
Supply voltage	1.8V
Bias voltage	1.8V
PSSR	85dB
CMRR	90dB

5. CONCLUSION

In this paper we present a simple Operational Transconductance Amplifier (OTA) topology for low voltage and low power applications, also operational transconductance amplifier (OTA) is one of the most significant buildings-blocks in integrated discrete-time filters used in analog to digital

converter (ADC) for Sigma-delta converter. Therefore, this operational amplifier can be used in low power also low voltage and high time constant applications such process controller also uses physical transducers and small battery operated devices. Hence, this work can be used in filter design, as (ADC) analog to digital converter design and instrumentation amplifiers as good purpose because of its high gain, high common mode rejection ratio (CMRR) and low power consumption.

6. ACKNOWLEDGEMENT

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REFERENCE:

[1] J. H. Botma, R. F. Wassenaar, R. J. Wiegerink, "A low voltage CMOS Op Amp with a rail-to-rail constant-gm input stage and a class AB rail-to-rail output stage", IEEE 1993 ISCAS, Chicago, pp.1314-1317.

[2] Paul R. Gray, Paul L. Hurst, Stephan H. Lewis and Robort G. Mayer "Analysis and design of analog integrated circuits", Forth Edition, John Wiley & sons, inc.2001, pp.425-439.

[3] Jung, W.G., IC Op-Amp Cookbook (Howard W. Sams -Bobs Merrill First Ed. 1974) p. 440 et seq.

[4] Vikram Palodiya, Shweta Karnik, Mayank Shrivastava and Itendra Dodiya, Design of Small-Gm Operational Transconductance Amplifier in 0.18µm Technology‖ International Journal of Engineering Research & Technology (IJERT) Vol. 1 Issue 5, July – 2012, ISSN: 2278-0181.

[5] Siddharth Seth and Boris Murmann ―Settling Time and Noise Optimization of a Three-Stage Operational Transconductance Amplifier ‖ IEEE transactions on circuits and systems—i: Regular papers, vol. 60, no. 5, May 2013

[6] Rekha S. and Laxminidhi T. ―A Low Power, Fully Differential Bulk Driven OTA in 180 nm CMOS Technology ‖ International Journal of Computer and Electrical Engineering, Vol. 4, No. 3, June 2012

[7] Majid Memarian Sorkhabi and Siroos Toofan, ―Design And Simulation of High performance Operational Transconductance Amplifier‖, Canadian Journal on Electrical and Electronics Engineering Vol. 2, No. 7, July 2011.

[8] Bhavesh H. Soni, Rasika N. Dhavse, ―Design of Operational Trans-conductance Amplifier Using 0.35µm Technology‖, International Journal of Wisdom Based Computing, Vol. 1(2), August 2011.

[9] Reetesh V. Golhar and Mahendra A. Gaikwad and Vrushali G. Nasre, ― Design and Analysis of High Performance Operational Transconductance Amplifier‖, International Journal of Scientific and Research Publications, Volume 2, Issue 8, August 2012.

[10] R. Nguyen and B. Murmann, ―The design of fast-settling two stage amplifiers using the open-loop damping factor as a design parameter,‖ IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no.6, pp. 1244– 1254, June, 2010

[11] Adel S. Sedra, Kenneth C.Smith "Microelectronic Circuits", Oxford university press, Fourth edition, 2002, pp.89-91.

[12] Jin Tao Li, Sio Hang Pun, Peng Un

Mak and Mang I Vai "Analysis of Op -Amp Power-Supply Current Sensing Current-Mode Instrumentation Amplifier for Biosignal Acquisition System", IEEE conference,August-2008, pp.2295-2298.

[13] Y. Tsividis, Operation and Modeling of the MOS Transistor, 2nd ed. Boston, MA: McGraw-Hill, 1998.

[14] D. A. Johns and K. Martin, Analog Integrated Circuit Design. New York: Wiley, 1997.

[15] Phillip E. Allen and Douglas R. Holberg "CMOS analog circuit design", second edition, Oxford university press, 2007, pp. 269-274.