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Parallel Distributed Arithmetic Technique for Discrete Wavelet Transform, Low Latency & High Throughput

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Abstract—Wavelet Transform is an important aspect in today's communication world, and widely used in the field of signal processing. Efficient architectures is implementation to get high throughput and low latency. Due to the demand for portable devices and real-time applications, the design has to be realized with very low power consumption and a high throughput. We will illustrate DWT using parallel DAT design which gives better results. Also, simulation results are obtained using Model sim which shows accepted outcomes.

Keywords:—DAT, discrete wavelet transform, filters, Model-sim, latency, throughput, matlab.

1. INTRODUCTION

Objective—**Project** significance / **Relevance** with ongoing academic activities:-

Our aim is to establish better results which leads to low latency and high throughput so that communication systems which is an important aspects in today's life can work more efficiently leading to customers satisfying qualities. The Wavelet Transform at high frequencies gives good time resolution and poor frequency resolution, while at low frequencies the Wavelet Transform gives good frequency resolution and poor time resolution.

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Figure 1. Time Frequency graph.

When Δt is large,

Bad time resolution

Good frequency resolution

When Δt is small,

Good time resolution

Bad frequency resolution

2. PROJECT IMPACT

Expected Outcomes:-

Parallel DAT when implemented results in increased speed as the input words reduces into smaller words and they proceeds parallel. As no. of parallel connection increases, throughput also increases. A fully parallel DA filter is achieved by factoring the input into single bit sub words achieves maximum speed. A new output will be computed every clock cycle which leads to high performance. Parallel Distributed Arithmetic Technique for Discrete Wavelet Transform, Low Latency & High Throughput Author (s) : Sara Varghese, Ptof. Utsav Malviya, G.G.I.T.S, Jabalpur

The two mean parameter her are latency and throughput which are describe below:

Latency: it is the time taken by a signal to pass through a system. The difference between the applied input and corresponding output obtained.

Throughput: It is the no. of samples obtained in one second for a specified work.



Figure 2 : Block diagram of Parallel Distributed Arithmetic implemented

Thus we get better results in following fields:

- Increased speed
- High Throughput
- Low latency
- Multiresloution
- Low cost
- Excellent performances.

When a serial DAT is replaced by a parallel DAT the change in latency and throughput is shown below:

Table 1. Latency- Throughput variation inserial and parallel DAT.

T e c h - nique	Latency (clock cy- cle)	Throughput (samples/sec)
SDA	8	1.25 MHz
PDA	2	5 MHz

We see that the latency decreases and throughput increases in parallel DAT which is desirable and will lead to better performance.

Distributed Arithmetic technique is used to compute the inner product equation in many applications. The inner SOP are arranged which in turn reduces MAC operations. Thus larger area occupied by multipliers are replaced by small tables. This reduces the hardware to a great level.

Daudechies filters provide many desirable results and therefore these are used here. It is suitable for compression applications and it provides perfect reconstruction conditions.

3. LITERATURE SURVEY

National And International Scenario:-

R.A. Harley solved the problem of increased power dissipation by applying pipelining techniques in DF filters.

Marino implemented both polyphase and pipelining so that low power and high speed is obtained. Transpose Form filters were used for the same which reduce critical delay but as a result latency was increased.

Polyphase architecture using Serial Distributed technique is implemented by Ali.M.Haj in Discrete Wavelets Transform. But this SDA architecture had large latency and low throughput because output depends on the number of bits of the input signal. Thus it is required that we implement / design architecture which provides high throughput and low latency. Parallel DAT is thus implemented.

10

Parallel Distributed Arithmetic Technique for Discrete Wavelet Transform, Low Latency & High Throughput Author (s) : Sara Varghese, Ptof. Utsav Malviya, G.G.I.T.S, Jabalpur

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11