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# Highly Speedy Floating ALU Design and Implementation on Course Grain FPGA

**Surya Kumar Chaturvedi**
*M. Tech. Scholar,*
*Shri Ram Institute of Technology*
*Jabalpur, (M.P) [India]*
*Email: schaturvedi326@gmail.com*

**Divayanshu Rao**
*Assistant Professor*
*Shri Ram Institute of Technology*
*Jabalpur, (M.P) [India]*

**Prof. Ravi Mohan**
*Associate Professor,*
*Department of Electronics & Communication Engg,*
*Shri Ram Institute of Technology,*
*Jabalpur, (M.P.) [INDIA]*
*Email: ravimohan7677@yahoo.co.in*

***Abstract:—*** *As we know that modern peoples are very much depends on digital systems it can have lots of examples ranging from i-pod, laptop, mobile phone, and computers to high speed super computers. All of these digital peripherals can be ASIC or Embedded system or Computer system. As every computer system or an embedded system requites computation and processing element to follow instructions, As the title explain proposed work is an implementation of highly area and speed optimised ALU. A Hybrid FPGA is differ than normal CPLD and it has in build optimised component that is the reason that thesis work has chosen hybrid FPGA to implement the proposed ALU. Proposed ALU uses Ancient Egyptian Multiplication for floating numbers and also proposed a tree addition in it. The observed results are 10% area and 7% speed optimised than previous work. Designing is done with the help of Xilinx EDA tool.*

***Keywords:—****Field Programmable Gate Arrays (FPGAs), Complex Programmable Logic Design (CPLD), Electronic Device automation (EDA), Integrated Simulation Environment (ISE)*

## 1. INTRODUCTION

The Egyptian way for representing numbers, it is the symbols for Egyptian numbers system. it is a description of what they signify, when numbers gets multiplying are long numbers in the number system, it is multiplying numbers by ten or hundred, and with present decimal numbers system it is very simple one just place the correct number of zeroes in the last. And it was not simple for the Egyptians

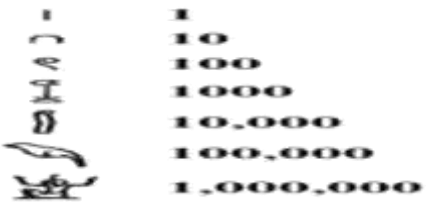


*Figure 1: Egyptian number system*

They require have had to modify all their symbols to the next one, or some more, so the finger came to the tadpole, and carried on. But, the Egyptians were also had different way of multiplying which was very good. All they had to do multiply and divide by two (2). This was simpler for them as compare to us, because half of symbol eight is four of a symbol all they have to mind is that half a tadpole is five

fingers, That is how they multiply 18 by 85 one can use this method in our number system, so one can follow their technique. One have to divide first number (here: 18) by 2 many times so it reach one. Few times one can-not, obviously, if one had an odd number, so one can subtract 1 before halving it. One must multiply the other number by 2 the same times.

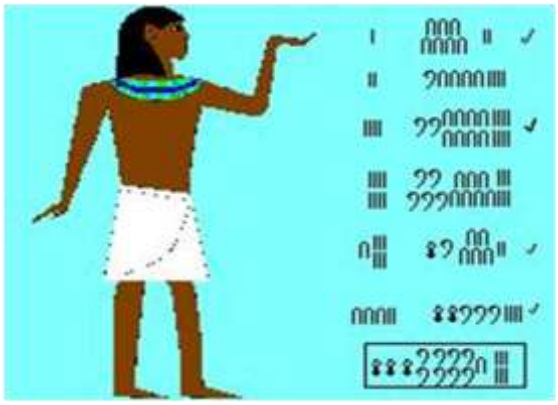

*Figure 2: Egyptian Multiplication*

Every time where one got the spare 1, must note what the doubled number and one simply add these numbers together, do not caring the others. This, tough to believe, is the same when the two numbers multiplied together, without even using multiplication tables and all. Figure 2 above show how Egyptian multiply. The figure 3 below is the our way to use Egyptian multiplication .

| 18 | × | 85 | = | 1530 |
|---|---|---|---|---|
| 1 | | 85 | | |
| 2 | | 170 | | 170 |
| 4 | | 340 | | |
| 8 | | 680 | | |
| 16 | | 1360 | | + 1360 |
| | | | | 1530 |

*Figure 3: Decimal multiplication with help of Egyptian technique*

## 2. LANGUAGE AND TOOLS USED

VHDL can say a versatile and very powerful HDL which can be useful for modelling many digital systems at every levels of design abstraction.

The ISE Design Suite is the popular electronic design automation (EDA) tool family sold by Xilinx. The ISE Design Suite advantage include RTL design entry and synthesis which supports VHDL or Verilog, place-and-route (PAR), full verification and debug and creation of the bit files that are used to configure the chip.

The ISE software controls all aspects of the design flow. Through the Project Navigator interface, you can access all of the design entry and design implementation tools. You can also access the files and documents associated with your project.

## 3. IMPLEMENTATION

As we have proposed to design a FPU unit for that we have to aware about the floating numbers and must keep in mind that computation for floating number is different the computation for non floating numbers, as our FPU design is for 16 bit numbers so we have taken the upper 10 bit out of 16 bit number as integer and remaining lower 6 bit of 16 bit number as float. An example is below:

| | | |
|---|---|---|
| 13.25 | => | 0000001101.010000 |
| | | 13 . 25 |
| 35.6875 | => | 0000100101.101100 |
| | | 35 . 6875 |

*Figure 4: proposed floating number*

This example shows peasant multiplication to multiply 11 by 3 in decimal format to arrive at a result of 33.

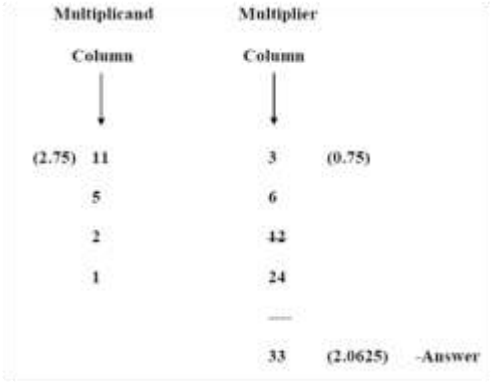


*Figure 5: the Egyptian multiplication in floating numbers*

***Describing the steps explicitly:***

- There are two columns; Multiplicand column & Multiplier column.
- If 11 is Multiplicand and 3 Multiplier, they are written under Multiplicand column & Multiplier column respectively.
- Half of 11 is 5.5 and 3 is doubled as 6. The fractional portion is discarded so 5.5 becomes 5.
- Half of 5 is 2.5 and 6 is doubled 12. The fractional portion is again discarded 2.5 becomes 2. The figure in the left column number 2 is even, so the figure in the right column 12 will not minded.
- Here, "t1 t2 t3", "t4 t5", "t6" are binary variables arranged in a tree form; Sx and Cx are Sum and Carry respectively.

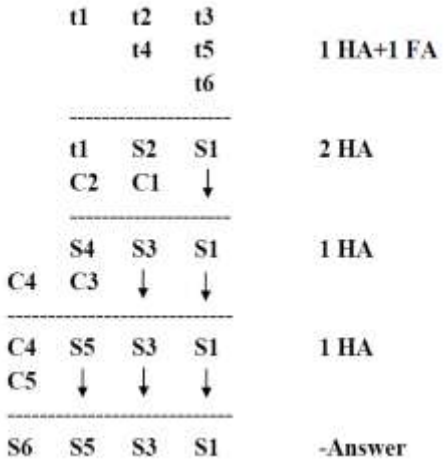


*Figure 6 : proposed Adder in Egyptian multiplication*

**Table 2: comparison of proposed adder with available adder structure**

| Logic Gate | Conventional Adder | Proposed Adder Tree |
|---|---|---|
| XOR | 18 | 14 |
| AND | 18 | 14 |
| OR | 8 | 2 |

## 4. RESULTS

**Table 3: Area & delay Estimates for Proposed Multipliers**

| No. of Slices | ***128*** |
|---|---|
| **No. of 4 Bit LUT** | 321 |
| **IOBs** | 70 |
| **Power Quiescent** | 333 mw |
| **Delay** | 10.642 ns |
| **Max. Freq.** | 93.967 MHz |

Table show the results which are been observed for the proposed multiplication of two 16 bit numbers as can observe that is requires only 321 slices and it works on 94 M. hz frequency as it is better than other work when area concerns.

## 5. CONCLUSION

Proposed work estimated the number of slices and 4 input LUTs is decreased by using Peasant Multiplication Algorithm and Addition Tree. I have come to a conclusion that our design for Floating Point Unit in Hybrid FPGA in which we are using Peasant Multiplier for multiplication purpose and proposed Adder Tree requires lesser amount of area (gates) & delay (ns) as compared to the reference base papers. These two techniques are able to decrease the area up to a great extent by increasing the Power.

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