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Multi-Threshold CMOS Design for Low Power 10T Full Adder

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Abstract*—Full Adder is the basic components of arithmetic and logic units of microprocessors. Improvement of this circuit would impart a greater impact on the performance of large systems where it has been employed. To improve the power consumption of the Full Adder the 10T structure has been utilized with MTCMOS technique at 45nm technology. Multi-threshold CMOS is popular circuit technique that enables high performance and low power operation. The paper here illustrates the analysis of leakage current active power, and delay with power supply of (0.7 V). The reduction in power consumption in the structure represented is computed as 39.20 nW and propagation delay of 10.51 ns, which significantly improves and makes the circuit highly energy efficient and optimization can be achieved between power and delay. The leakage current has been reduced to 18.21 nA with power supply of 0.5v to 0.9v. The adder has been analyzed for various parameters. The simulation here has been done using the cadence virtuoso tool.*

Keywords:— *Full Adder, Low Power, CMOS Circuit, MTCMOS technique.*

1. INTRODUCTION

Full adder is the fundamental unit in circuits used for performing arithmetic operations such as compressors, comparators, multipliers, and parity checkers [1]. Thus, enhancing the performance of the full adder block leads to the enhancement of the overall system performance [2]-[3]. Therefore, reducing power consumption in full adders, will reduce the overall power consumption of the whole system. Most of the VLSI applications, such as video processing, and microprocessors widely use arithmetic operations. There are several issues related to the full adders. Some of them are noise immunity power consumption, and good driving ability [4]. Several works have been done in order to decrease transistor count and consequently decrease power consumption and area [5]. Minimizing power dissipation is therefore important, both for increasing levels of integration and to improve reliability, feasibility, and cost [6]. An adder is one of the most critical components of a processor which determines its throughput and for address generation in case of memory access. The full adder performance would affect the system as a whole. A range of full adders using dynamic logic styles have been reported in the literature [7]. The reliability of the chip will be greatly degraded with high power dissipation due to silicon failure mechanism such as electro migration. The linear scaling of supply voltage with the feature size was started from half-micron technology. But the power supply scaling affects the speed of the circuit [8]. In order to maintain portability of high performance fidelity applications, emphasis will be on incorporation of low power modules in future system design. The design of such modules will have to partially rely on reduced power consumption and dissipation in fundamental arithmetic computation units such

as adders. Therefore, many efforts have recently done to implement high-speed and low-power 1-bit full adder cells with smaller area [9]-[10]. In this paper, we propose a systematic approach to design 10-transistor full adders. Our new adders also have the threshold -loss problem however; the adders are useful in larger circuits such as multipliers despite the threshold-loss problem.

2. REVIEW OF FULL-ADDER DESIGN

A one-bit full adder is a combinational circuit that performs the arithmetic sum of three bits. It consists of three inputs a, b, and c_{in} and two outputs S and Cout [11]. As illustrated in Figure 1. Expressions for S and Cout are given in (1) and (2).

$$S = a \oplus b \oplus c_{in} \quad (1)$$

$$C_{out} = a.b + b.c_{in} + c_{in}.a \quad (2)$$

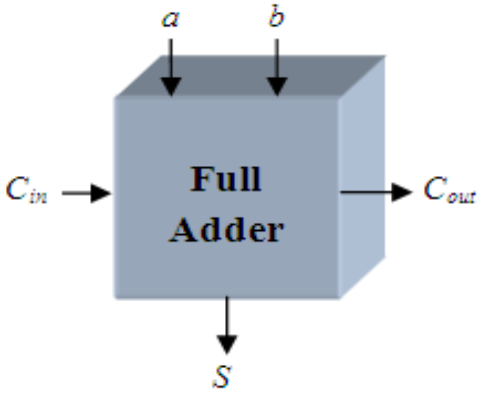

Figure 1: Block diagram representation of one-bit full adder.

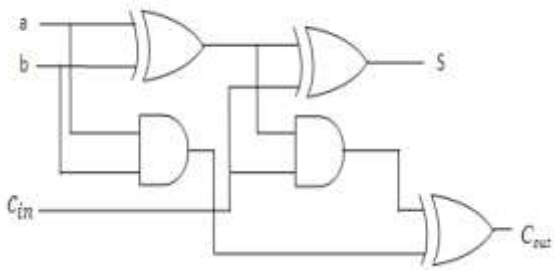

Figure 2: Schematic of a Full Adder.

The average power consumption in a generic digital CMOS gate is given as [12]:

$$P_{avg} = P_{dynamic} + P_{short-circuit} + P_{static} \quad (3)$$

$$= V_{DD} f_{clk} \sum_i (V)_{iswing} C_{iload} \alpha_i) + V_{DD} \sum_i I_{isc} + V_{DD} I_i \quad (4)$$

Where f_{clk} is the system clock frequency, V_{iswing} is the voltage swing at node i, C_{iload} is the load Capacitance at node i, α_i is the activity factor, I_{isc} is the short circuit current and Ii is the leakage current. usually CMOS devices in the subthreshold region, the power supply voltage is forever kept lower than the device threshold voltage. This conforms that the transistor channel is never fully inverted, but is consummate in weak or moderate inversion while the transistor is in its 'on' state. Due to the exponential V-I relationship, sub-threshold logic gates have a near ideal voltage transfer characteristics [13]. The V-I relation of the saturated device in weak inversion through the EKV model is expressed as [14]-[15].

$$I_{sub} = I_S . e^{\frac{V_G - V_{T0} - nV_S}{nU_T}} \qquad (V_{DS} > 4.U_T) \quad (5)$$

Where I_S is the specific current described by the model is:

$$I_S = 2.n.\eta_n(p).C_{ox}.\frac{W}{L}.U_T^2 \quad (6)$$

Note that all potentials are referred to the local substrate. U_T is the thermal voltage has a value of KT/q, VT0 is the zero-biased threshold voltage, n is the subthreshold swing parameter (slop factor), $\eta_n(p)$ is the carrier mobility for n or p channel devices, C_{ox} is the oxide capacitance, W is the effective width and L is the length of the channel.

14T Full Adder

The 14T adder with 14 transistors consumes considerably less power in the order of microwatts and has higher speed. The 14T

adder reduces threshold loss problem compared to the previous different types of transistor adders. In future, this kind of low power and high speed adder cell will be used in designing the digital FIR filter and its applications in various fields. On the other hand, increasing demand for portable equipments such as cellular phones, personal digital assistant (PDA), and notebook personal computer, arises the need of using area and power efficient VLSI circuits [16]. New-14T, Figure 3 is an improvement from 14T [17]. Which has simultaneous XOR and XNOR signals? Feedback transistors provide rail-to-rail outputs in XOR-XNOR module. However, they prompt high delay.

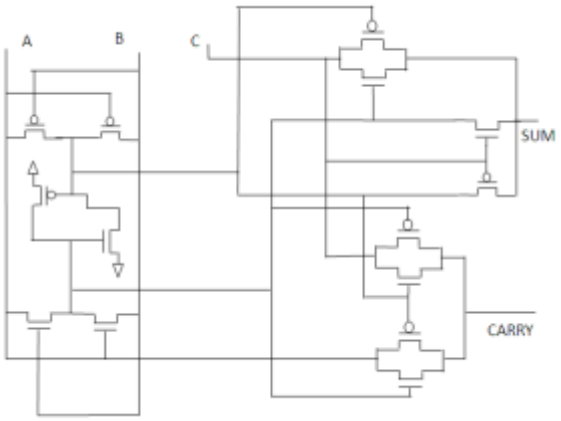

Figure 3: Schematic of 14T Full Adder 45nm technology

Transistor circuit that also produces a complementary XNOR output is introduced in the general Full Adder. The 14T full adder cell, like the transmission function full adder cell, implements the complementary pass logic to drive the load. New design eight other designs, including Hybrid and three previous majorities not based Full Adder designs are applied. Simulation results illustrate improvements in terms of delay [18]. The SERF design requires only 10 transistors to realize the adder function. Even though it has threshold loss problem, it is suited for low power design so far. As mentioned earlier, the performance of many larger circuits are powerfully dependent relative on the performance of the full adder circuits that have been used. The new enhanced 14-transistor adder circuits obtainable in this study are good candidates to put together these large systems, such as high performance multipliers with low power consumption. The small enhance in Transistor count of these adders can considerably decrease the Latency of the systems built upon them.

10T Full Adder

In this study we investigated the power and delay performance characteristics of adder using 10-transistor adder circuits. The basic benefit of 10 transistors full adders [19]-[20]. In pass transistor logic the output voltage swing may be degraded due to the threshold voltage overcome problem. The reduction in voltage swing leads to lower power consumption but may also lead to slow switching in the case of cascaded operation such as ripple carry adder. A low VDD operation the corrupted output may even cause break down of circuit [21]. The smallest voltage that 10 T adder can work at 0.7V. The excessive power dissipation and long delay are attributed to the threshold voltage drop problem and the poor driving capability of some internal nodes at input combinations that create non full-swing transitions [22]. The designed 10T full adder shown in figure 4.

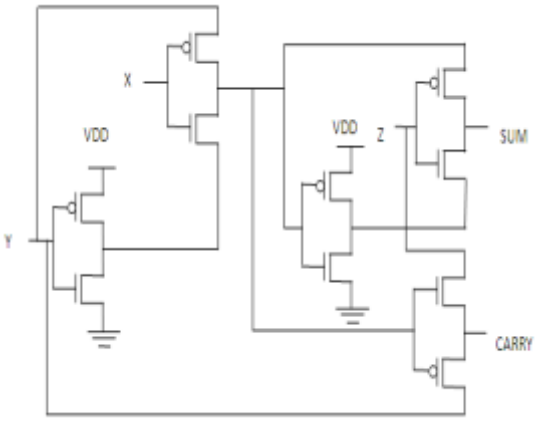

Figure 4: Schematic of 10T Full Adder 45nm technology

The adder circuit is designed using the transmission gates, which decrease the number of transistors required for the addition. The multiplier is designed using the transmission-

gate based adder, 10T adder and latch adder. Adder is one of the most important components of a CPU (central processing unit), Arithmetic logic unit, floating point unit and address generation like cache or memory access unit use it. In addition, Full adder is important component in other applications.

3. MTCMOS TECHNIQUE

In MTCMOS technique, transistors of low threshold voltage become disconnected from power supply by using high threshold sleep transistor on the top and bottom of the logic circuit. Transistor having low threshold voltage (low-Vth) is used to design logic as shown in figure 5. The sleep transistors are controlled by the sleep signal. During the active, the sleep signal is disserted, causing both high Vt transistor to turn on and provide a virtual power and ground to the low Vt logic. When the circuit is inactive sleep signal is asserted forcing both High Vt transistor to cut-off and disconnect power lines from the low Vt logic. The transistors having high threshold voltage are used to isolate. In this technique, a sleep transistor is added between the actual ground rail and circuit ground called virtual ground [23]. The MTCMOS method has become very popular and there has been significant research towards optimizing its benefits [24]. A popular low leakage circuit technique is the Multithreshold Voltage CMOS (MTCMOS). One drawback of this method is that portioning and sizing of sleep transistors is difficult or large circuits. The multi threshold CMOS technology has two main features. First, "active" and "sleep" operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip. This technique based on disconnecting the low threshold voltage (low-Vt) logic gates from the power supply and the ground line through cut-off high threshold voltage (high-Vt) sleep transistors is also known as power gating. The schematic of power gating technique using MTCMOS is shown in Figure 5. The transistors having low threshold voltage are used to implement the logic. MTCMOS technology has emerged as a promising alternative to build logic gates operating at a high speed with relatively small power dissipation as compared to traditional CMOS.

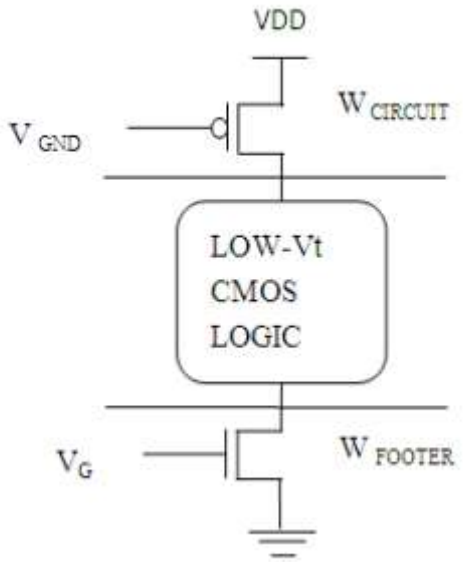

Figure 5: We call this power gating approach fine-grained power gating.

Let us consider that the footer device operates in the weak inversion region (VG < VTH) and the leakage of the logic circuit can be approximated by the leakage of a single transistor of effective width Wcircuit as shown in Figure 5. Under the assumption that the footer is biased in the weak inversion region, the steady state VGND potential can be obtained by matching the leakage current of the logic circuit with the leakage of the footer device.

$$I_{leak}\,(Circuit) = I_{leak}\,(Footer) \quad (7)$$

Substituting

$$I_{leak} = I_0 \left(\frac{W}{L}\right) 10^{\frac{(V_{GS} - V_{TH}) + \eta(V_{DS})}{S_S}}$$

for the logic circuit and the footer

$$I_0 \frac{W_{CIRCUIT}}{L} 10^{\frac{(-V_{THC}) + (V_{DD} - V_{GND})}{S_S}} = I_0 \frac{W_{FOOTER}}{L} 10^{\frac{(V_G - V_{THF}) + \eta(V_{GND})}{S_S}} \quad (8)$$

Here, V_{THC} and V_{THF} represent the threshold voltages of the logic circuit and the footer device respectively, η is the DIBL

coefficient and S_S is the Subthreshold slope. Solving Equation 8 for V_{GND} results in following expression:

$$V_{GND} = \frac{-V_G + S_S \log_{10}\left(\frac{W_{CIRCUIT}}{W_{FOOTER}}\right) + (V_{THF} - V_{THC}) + \eta V_{DD}}{2\eta} \quad (9)$$

The above equation shows that the steady state V_{GND} is linearly dependent relative on footer gate voltage V_G with a negative slope. If the footer gate voltage is better, it results in a reduce in the virtual ground potential. Therefore, V_{GND} potential in the sleep mode can be efficiently controlled by the gate voltage of the footer.

$$\frac{I_{sleep}}{I_{active}} = 10^{-\left[\frac{\eta(V_{DD} - V_{GND})}{S_S}\right]} \quad (10)$$

Simulation Results of 14 Transistors

We have performed simulated results using spectre simulator in cadence tool at 45 nm technology. The supply voltage is 0.7v (45nm). The output waveform of 14T full adder simulated at 45 nm technology under the process of transient analysis for the period of 100ns and power supply of 0.7 V.

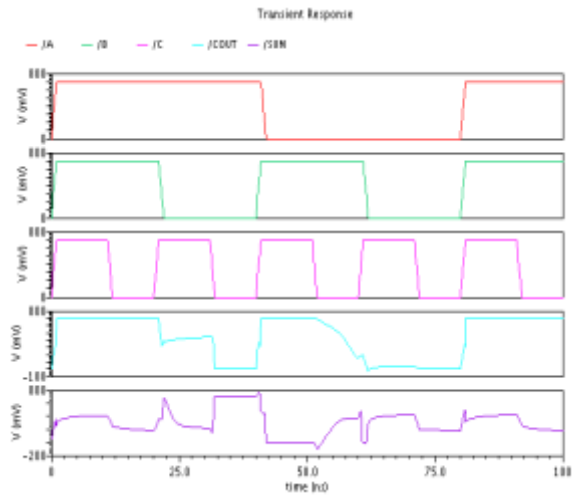

Figure 6: Simulated output waveform of transient response 14T 45nm technology.

Figure 7 shows the output waveform of leakage current of 14T full adder simulated at 45nm technology under the process of transient analysis for the period of 100ns and power supply of 0.7 V. Leakage current is also the current that flow when the ideal current is zero, such as in electronic assembly that are in stand by disabled or "sleep" mode.

$$P(V_t) = V_{cc} I_{off}(V_t) \quad (11)$$

Where, $P(V_t)$ = leakage power, V_{CC} = applied voltage and I_{off} = leakage current

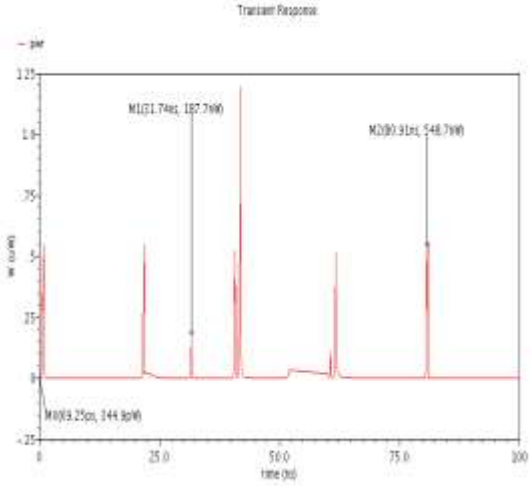

Figure 7: Simulated output waveform of leakage current 14T at 45nm technology.

Figure 8 shows the output waveform of active power simulated at 45nm technology under the process of transient analysis for the period of 100ns and power supply of 0.7V.

$$P_{avg} = C V_{DD}^2 f_{CLK} \quad (12)$$

Where, P_{avg} = Average Power, C = load capacitance and f_{CLK} = clock frequency.

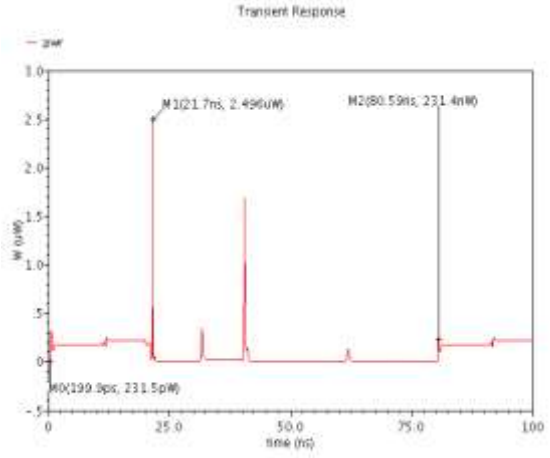

Figure 8: Simulated output waveform of active power 14T at 45nm technology.

Simulation Results of 10 Transistors

We have performed simulated results using spectre simulator in cadence tool at 45 nm technology. The supply voltage is 0.7v (45nm). The output waveform of 10T full adder simulated at 45 nm technology under the process of transient analysis for the period of 100ns and power supply of 0.7 V.

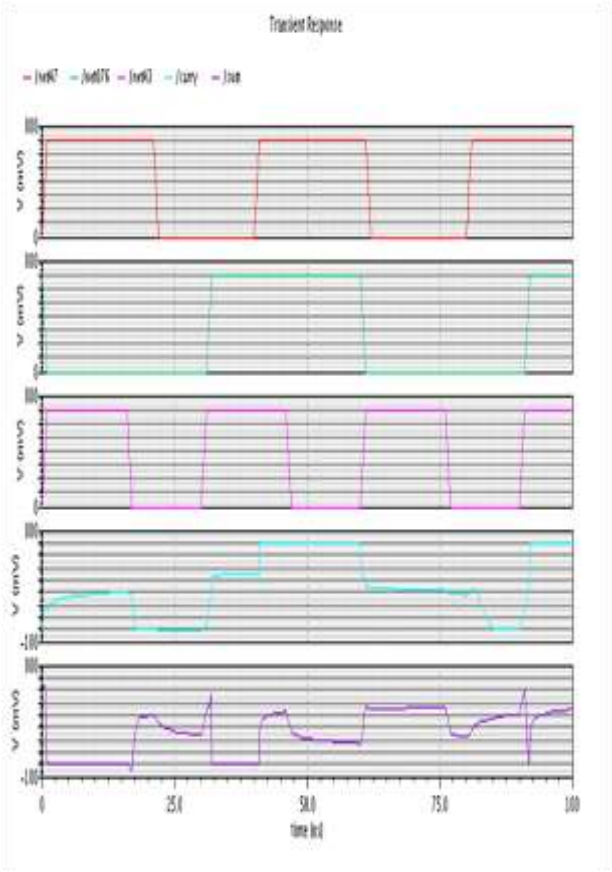

Figure 9: Simulated output waveform of transient response 10T 45nm technology.

Figure 10 shows the output waveform of leakage current of 10T full adder simulated at 45nm technology under the process of transient analysis for the period of 100ns and power supply of 0.7 V. Leakage current is also the current that flow when the ideal current is zero, such as in electronic assembly that are in stand by disabled or "sleep" mode.

$$P(V_t) = V_{cc} I_{off}(V_t) \quad (13)$$

Where, $P(V_t)$ = leakage power, V_{CC} = applied voltage and I_{off} = leakage current

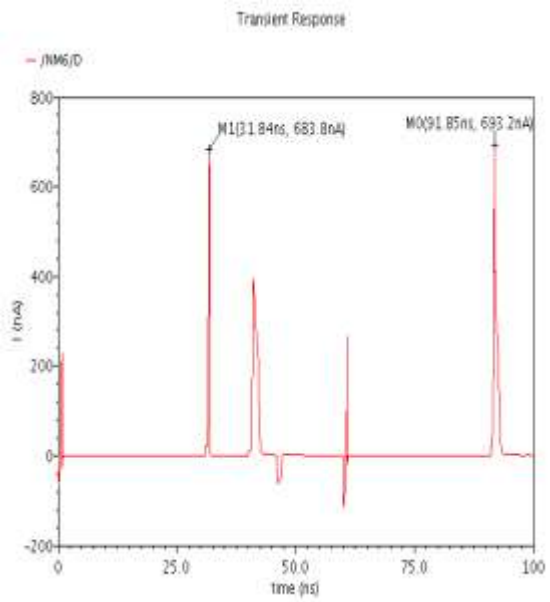

Figure 10: Simulated output waveform of leakage current 10T at 45nm technology.

Figure 11 shows the output waveform of active power simulated at 45nm technology under the process of transient analysis for the period of 100ns and power supply of 0.7V.

$$P_{avg} = CV_{DD}{}^2 f_{CLK} \quad (14)$$

Where, P_{avg} = Average Power, C = load capacitance and f_{CLK} = clock frequency.

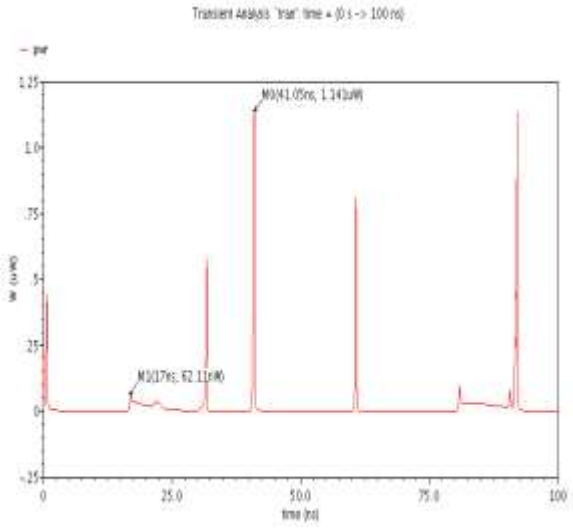

Figure 11: Simulated output waveform of active power 10T at 45nm technology.

Figure 12: shows the output waveform of leakage current of 10T full adder using MTCMOS technique simulated at 45nm technology under the process of transient

analysis for the period of 100ns and power supply of 0.7 V. Leakage current is also the current that flow when the ideal current is zero, such as in electronic assemblies that are in stand by disabled or "sleep" mode.

$$P(V_t) = V_{cc} I_{off}(V_t) \quad (15)$$

Where, $P(V_t)$ = leakage power, V_{CC} = applied voltage and I_{off} = leakage current

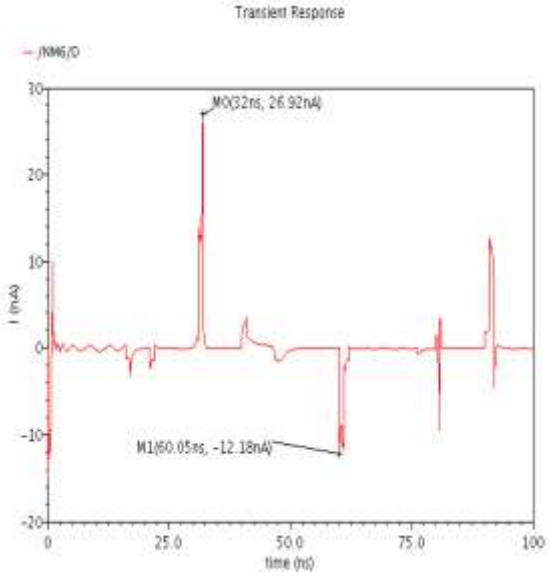

Figure 12: Leakage Current of 10T full adder using MTCMOS Technique at 45nm technology.

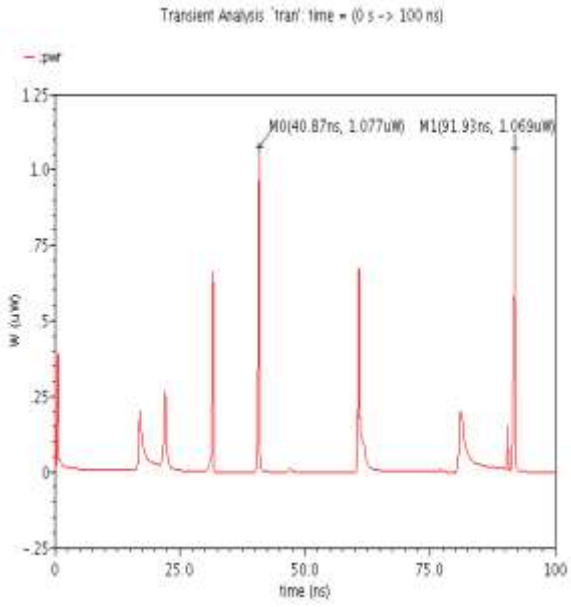

Figure 13: Active Power of 10T full adder using MTCMOS Technique at 45nm technology.

Figure 13: shows the output waveform of active power simulated at 45nm technology under the process of transient analysis for the period of 100ns and power supply of 0.7V.

$$P_{avg} = CV_{DD}{}^2 f_{CLK} \quad (16)$$

Where, P_{avg} = Average Power, C = load capacitance and f_{CLK} = clock frequency.

4. RESULT AND DISCUSSION

Table 1 shows the simulation results for 14T Full adder and 10T Full Adder Performance comparison regarding power, leakage current, and delay and power delay product. All the Full Adders were supplied with two different technologies.

Table 1 : Simulation result of 14T and 10T Full Adder with MTCMOS Technique

Technology	Voltage (V)	Active Power (µW)	Leakage Current (µA)	Delay	PDP
14T Full Adder	0.7	48.89	22.39	15.67	764.69
	0.9	52.07	25.77	18.01	937.77
14T Full Adder Using MTCMOS	0.7	41.89	20.34	12.11	507.28
	0.9	48.33	21.32	13.01	628.77
10T Full Adder	0.7	39.20	18.02	10.51	411.99
	0.9	41.61	21.54	11.31	470.60
10 T Full Adder Using MTCMOS	0.7	24.26	0.707	0.736	17.811
	0.9	92.03	0.472	0.129	11.043

Table: 2 shows the simulation results for 10T Full adder Performance comparison regarding power, leakage current, and delay and power delay product. All the full adders were supplied with two different technologies. As the temperature increases the minority carriers are generated in base collector region,

since more bands are broken, the leakage current increases.

Table 2 : Simulation result of 14T and 10T Full Adder USING Temperature (◦c)

Tech-nology	Tem-perature (◦c)	Active Power (µW)	Leakage Current (µA)	Delay	PDP
14T Full Adder	50	40.12	8.204	3.867	155.14
	75	43.65	7.653	4.010	175.03
14T Full Adder Using Mtcmos	50	38.56	4.178	2.001	77.15
	75	41.87	4.989	1.996	83.57
10T Full Adder	50	36.89	3.056	1.034	38.14
	75	42.34	3.984	2.358	99.83
10 T Full Adder Using MTCMOS	50	27.23	0.837	0.676	18.40
	75	33.12	0.981	0.639	21.16

5. CONCLUSION

Calculation of 14T Full Adder and 10T Full Adder various parameters has been at 45nm technology and compared with MTCMOS technique. 14T Full Adder and 10T Full Adder has been analyzed at various temperatures for obtaining power performance. The active power has been calculated at 45nm technology using Cadence Virtuoso Tool. Simulation results show that power consumption of the circuit is reduced to 89.2nW for 0.7V at 45nm and reduces further on reduction of the supply voltage. Delay has also been improved and reduced to 08.23ns at 0.7V at 45nm technology. The comparison shows that the implementation of the 10T full adder using power gating technique would be better at 45nm technology as compared to 10T full adder. The results confirm that MTCMOS technique reduces the power significantly and makes the circuit suitable for practical applications.

6. ACKNOWLEDGMENT

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