ISSN 2320-9984

Volume 2 Issue 1 | March 2014 ISSN: 2320-9984 (Online)

International Journal of Modern Engineering & Management Research

Website: www.ijmemr.org

An approach of Vedic Multiplication Technique for Optimising Logic Delay in MAC Unit

Nidhi Rajput
Research Scholar
Department of Electronics and Communication Engg.
Takshshila Institute of Engineering and Technology,
Jabalpur, (M.P.) [INDIA]
Email : nidhirajput1991@gmail.com

Prof. Rakesh Patel
Associate Professor & Guide,
Department of Electronics & Communication Engg,
Takshshila Institute of Engineering and technology,
Jabalpur, (M.P.) [INDIA]
Email : rakeshpatel04@gmail.com

Abstract*—The multiplier is the key element of all these processor like Microprocessor, Microcontroller, DSP processor etc. Now a days we are living in digital world, where all the operations get performed more reliably and with highest accuracy by digital signal processor. After through study and deep analysis work we have seen that the existing Vedic multiplication hardware has some limitation in terms of area To overcome these limitations a novel approach has been proposed to design the Vedic multiplier with unique addition structure, which is used to add partially generated products. To meet major concern 'Speed' it is needed particular high speed multiplier, the speed of multiplier greatly depends upon the type of multiplication technique used in it. The proposed is an idea to merge two different multiplication techniques Vedic and Tree addition structure and these gives us a fast and area efficient multiplication approach.*

Keywords:—*Arithmetic and Logical Unit (ALU), Digital Signal Processor (DSP), Field Programmable Gate Array (FPGA), Multiply and Accumulate (MAC), Multiplier.*

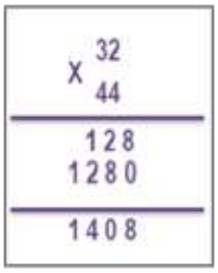
1. INTRODUCTION

ALU is the key element of Microprocessors, Microcontrollers and embedded systems. Multiplication is one of the prime requirements of any ALU designing & multiplication is known as MAC[3] in modern DSP Processor [6], Microprocessors & Microcontroller, the method which we choose for designing MAC will affect Microprocessor or Microcontroller performance.

1.1 Conventional Multiplication

Multiply 32 with first RHS digit 4 = 128. And store it in register. Then multiply second RHS digit 4 with 32 = 128. Provide shifting of 1 digit = 1280.

Add first partial product with second. And get result.



1.2 Vedic Multiplication (Urdhva Triyambakam sutra)

The multiplier is based on an algorithm Urdhva Triyambakam (Vertical & Crosswise) of ancient Indian Vedic Mathematics[8]. Urdhva Triyambakam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise"[4].

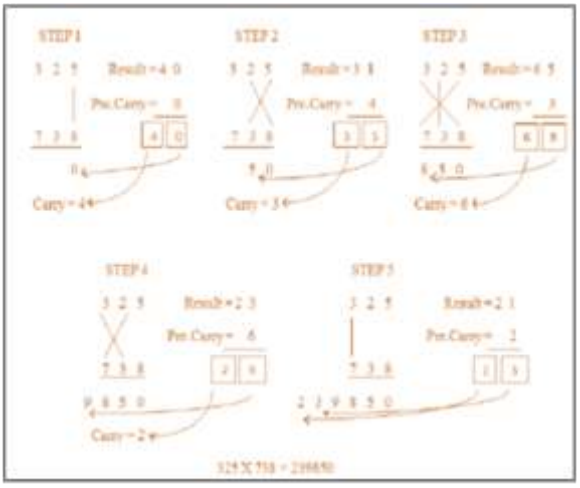


Figure 1: The Method of Urdhva Triyambakam

Figure 1 shows multiplication of two decimal numbers- 325*738 by Urdhva Triyambakam method[2]; to illustrate this multiplication scheme let us consider the multiplication of two decimal numbers (325 * 738). The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel [5][7], the multiplier is independent of the clock frequency of the processor[1]. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies.

2. METHODOLOGY

2.1 Structure of Design

To design Vedic multiplier we need to design major blocks of the complete application, paper work has design a 4 bit Vedic MAC which is actually proposed research design module and then paper work have design 16 bit Vedic MAC using 4 bit Vedic MAC, after designing 16 bit MAC paper work have design 16 bit logical module to perform all logical operations. At the end paper work did integration of 16 bit MAC with 16 bit logical module.

2.1.1 The top module

Figure 2 shown below is the top module of our design structure tree; it has two components 16 bit MAC and 16 bit Logical block.

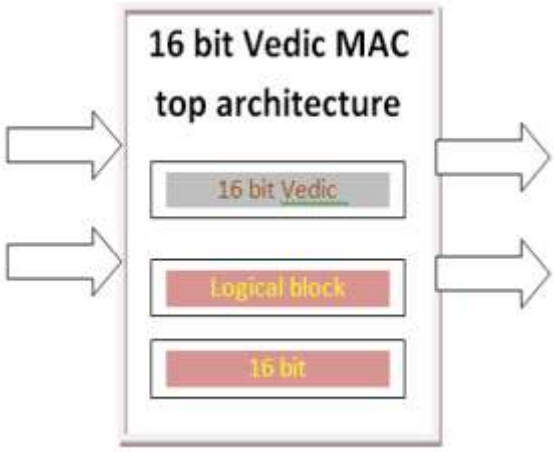


Figure 2 : Top Design Module of Vedic ALU

2.2 The 16 bit MAC

Figure 3 shown below is the design of our proposed 16 bit MAC it has used sixteen 4 bit Vedic MAC to perform computation on 16 bit input numbers.

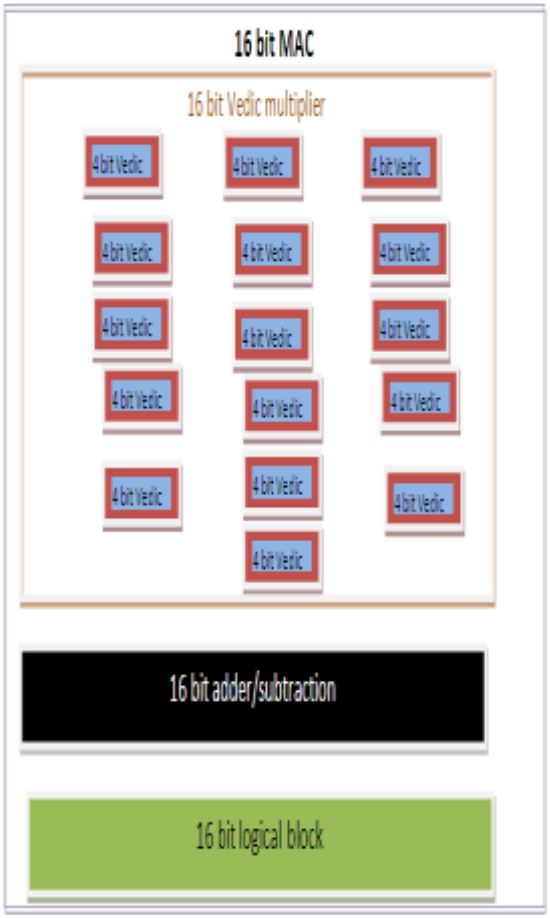


Figure 3- 16 bit Vedic MAC (Multiply and accumulate)

2.3 The 4 bit MAC

In the program entity "vedicmau" is the 4 bit MAC (Multiply and accumulate)

In1 & In2 are the 4 bit numbers, below is the explanation of 4 bit vedic MAC

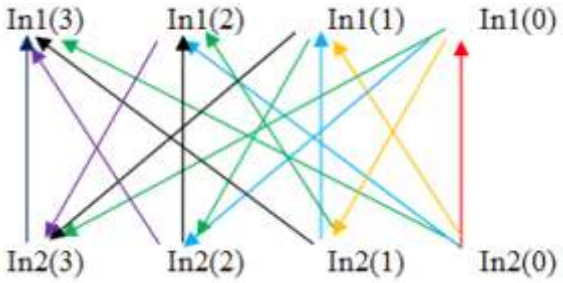


Figure 4: 4 bit MAC (Multiply and accumulate)

In Figure 4 above every arrow is the 'AND' operation

- The red produce "t1"
- The yellow produce t2 & t3
- The light blue produce t4 & t5 & t6
- The green produce t7 & t8 & t9 & t10
- The black produce t11 & t12 & t13
- The purple produce t14 and t15
- The dark blue produce t16

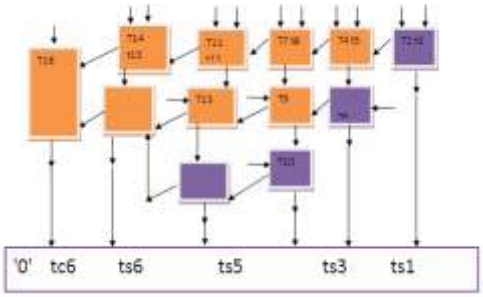


Figure 5: A New Carry Save Addition Approach

Figure 5 shows the multiplication result for 4 bit MAC unit 8 bit result of multiplication of two 4 bit inputs is:

0_tc6_ts6_ts5_ts3_ts1_t3_0

2.4 16 bit MAC

Now for 16 bit multiplication, paper work have 16 bit inputs x & y and answer will be produce in z which will be of 32 bit. paper work perform "4 bit multiplication "on each arrow as shown in figure below.

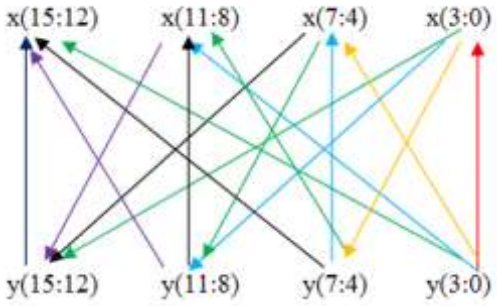


Figure 6 : 16 bit MAC (Multiply and accumulate)

- red arrow multiplication produce 8 bit ans. [om11:ol11]
- yellow arrow multiplication produce 8 bit ans. [om21:ol21], [om22:ol22],
- blue arrow multiplication produce 8 bit ans. [om31:ol31], [om32:ol32], [om33:ol33]
- green arrow multiplication produce 8 bit ans. [om41:ol41], [om42:ol42], [om43:ol43], [om44:ol44]
- black arrow multiplication produce 8 bit ans. [om51:ol51], [om52:ol52], [om53:ol53]
- purple arrow multiplication produce 8 bit ans. [om61:ol61], [om62:ol62],
- dark blue arrow multiplication produce 8 bit ans. [om71:ol71]

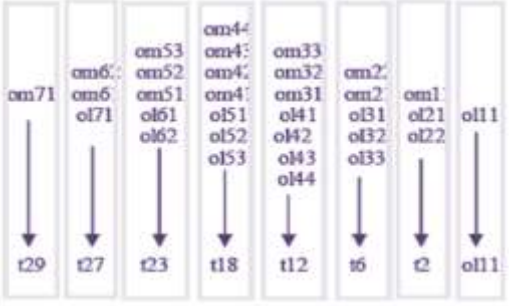


Figure 7 : Addition Structure for 16 Bit MAC

Proposed addition structure each of variable above shown above is of 4 bit. The addition of yellow boxes shown above results the multiplication of 16 bit numbers, and result is of total 32 bit.

3. RESULTS

Table 1: Results of Vedic 16 bit MAC (the complete design)

No of Slices	**466**
No of 4 input LUT	831
No of bounded IOBs	68
Logical Delay	9.007 ns

Table 2: Results of proposed 4 bit Vedic multiplier (paper work proposed Vedic design)

No of Slices	**19**
No of 4 input LUT	33
No of bounded IOBs	16
Logical Delay	7.947 ns

Table 3: Comparative results of with 4 bit multiplier

	Logical Delay	**Slice**
Proposed Vedic 4 bit multiplier	7.947 ns	19
Ref4	6.216 ns	27
Ref 5	-	25
Ref 3	10.95 ns	20

From tables above as can be observe that paper works are batter in aspect of area (i.e. less number of Slice) and speed (i.e. logical delay) in 4 bit MAC/multiplication as compare to base[3] paper.

Paper work is a design of 4 bit vedic multiplier (main actual research work) and use it to design 16 bit ALU. So paper work should make comparison with 4 bit vedic only, rest of comparison are just to make more precise comparison.

4. CONCLUSIONS

After actual implementation of proposed work the observed results are little low than expectation and the proposed work can be implemented with full custom at transistor level as proposed work is a semicustom at GATE level. A full custom will further increase the efficiency of proposed work in respect of Area, speed and power. The work can be design at more precise software tools like Synplyfy and more precise place and route can be done for much optimised speed and area. Above as can be observe that paper works are better in aspect of area (i.e. less number of Slice) and speed (i.e. logical delay) in 4 bit MAC/multiplication as compare to base[3] paper. Above as can be observe that paper works are better in aspect of speed (i.e. logical delay) in 8 bit as compare to base1, base2 & base3 papers. We have design 4 bit Vedic multiplier (main actual research work) and use it to design 16 bit multiplier. So paper work should make comparison with 4 bit Vedic only.

REFERENCES :

[1] M. Ramalatha, K. Deena Dayalan, P. Dharani, S. Deborah Priya," High Speed Energy Efficient ALU Design using Vedic Multiplication Techniques" ACTEA, July 15-17, 2009.

[2] Anvesh Kumar, Ashish Raman, "Low Power ALU Design by Ancient Mathematics", IEEE, Volume 5, 2010.

[3] Devika Jaina, Kabiraj Sethi, Rutuparna Panda, "Vedic Mathematics Based Multiply Accumulate Unit" International Conference On Computational Intelligence And Communication System, IEEE, 2011.

[4] M. Ramalatha,, K. Deena Dayalan,, P. Dharani,,S. Deborah Priya, "High Speed Energy Efficient ALU Design using Vedic Multiplication

Techniques" ACTEA 2009.

[5] Ramesh Pushpangana, Vineeth Sukumaran, Rino Innocent, Dinesh Salikumar, Vaisak Sundar,"High Speed Vedic Multiplier for Digital Signal Processors", IETE Journal for Research, Volume 55, ISSUE 6, Nov-Dec 2009.

[6] S. S. Kerur, Prakash Narchi, Jayashree C N, Harish M Kittur and Girish V A," Implementation of Vedic Multiplier for Digital Signal Processing", International Conference on VLSI, Communication & Instrumentation (ICVCI) 2011 Proceedings published by International Journal of Computer Applications® (IJCA)

[7] Umesh Akare, T. V. More, R. S. Lonkar," Performance Evaluation and Synthesis of Vedic Multiplier", National Conference on Innovative Paradigms in Engineering & Technology (NCIPET- 2012) Proceedings published by International Journal of Computer Applications® (IJCA).

[8] G. Ganesh Kumar, V. Charishma," Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques", International Journal of Scientific and Research Publications, Volume2, Issue 3, March 2012.