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Simulation and Analysis of DG-MOSFET for Ultra Low Power

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Abstract*—The low power consumption and good speed has become an important issues in the minds of consumers as electronic items are increasing in every houses, everyday. VLSI has been very successful in this aspect as new and new technologies are been developed in VLSI, which has lead, a solution to the above problem. DG MOSFET, proposed in 1984 as "XMOS" by ETL is the most promising and leading contender for nano regime devices. It has been expected to be the most advanced transistor giving a breakthrough to the scaling limit due to increasing leak current and short channel effects in the ordinary single- gate MOSFET. However, the conventional double-gate MOSFET with combined two gates held at an identical voltage has to work in a 3-terminal mode. The newly developed double-gate MOSFET can be driven in a genuine 4-terminal mode with independent two gates controlled separately. This means that the transistor operation speed can be controlled to an optimum, and the power loss caused by leak current during standby is substantially nullified. That is, the new technology will open the way to the implementation of the ultra-low power LSI characterized by optimum power control without sacrificing operation speed. The 4-terminal driven double-gate MOSFET can also be regarded as a MOSFET equipped with an arithmetic operation feature based on independent two-input reduction of the number of devices in VLSIs.*

Keywords*—DG Mosfet, threshold voltage, subthreshold swing, Mosfet scaling, DIBL, Drain Leakage Current (Ioff)*

Objective - Project Significance / Relevance with ongoing academic activities:-

With new and new technology coming in and new electronic devices been introduced very second, our aim is to get the best performance from these devices. In order to get better results we need to improve our object used and there parameters thus nullifying undesired outcomes, thus resulting in low power and good speed of the device.

We are aware that DG Mosfet can perform better than conventional devices like CMOS, MOS, etc.., Thus when DG Mosfet will replace the conventional objects in electronic devices we will get extremely better results. We just need to do variations with some of the parameters in order to get the desired outcomes and implement the same.

Previously, CMOS, MOS, or even conventional DG Mosfet were used in which both the gates where provided with same voltage. But when we provide both gates of DG Mosfet with different voltages we are able to control the channel with both sides and thus have better eelectrostatic control over the channel, so we can perform more scaling of gate length. Due to better control on short channel effects DG Mosfet is better alternative of conventional bulk MOSFET and it has higher current density, higher sub threshold

swing at low supply voltages. Thus we are able to maintain the device performance in terms of higher current density and low leakage by using DG Mosfet.

Project Impact - Expected outcome:-

Use of DG Mosfet in electronic device will help us to control important charactertics. They are as follows:

- Reduce Short Channel Effect (SCE)
- Sub Threshold conduction is low
- Ultra Low Power Consumption.
- Nullifies Leakage current.
- Consumes less area.
- Cost efficient.
- Best Power Conversion Efficiency.
- Increased Speed.
- Reliability

All these characteristics are helping us to improve our device by providing excellent outcomes.

Literature survey on National & International scenario:-

In January 2012, Santosh Kumar Gupta, Achinta Baidya and S. Baishya has published a paper entitled "Simulation and Analysis of Triple Metal Double Gate DG-MOSFET for Diminished SCE." In this paper they have used top and bottom gates with different work function to screen the effect of drain (DIBL effect). This results in improved carrier transport in the channel.

Also in January 2012, Vinay Kumar Yadav and Ashwani k. Rana has published a paper entitled " Impact of Channel Doping onn DG-Mosfet Parameters in Nano Regine." In this paper they have investigated the impact of channel engineering on double gate MOSFET by using different channel doping thereby leading to better results as short channel effects are reduced.

In 2011, Ramesh Vaddi, Rajendra P. Agarwal, Sudeb Dasgupta and Tony T.Kim published a paper on DG Mosfet regarding low lower in RFID. It talks about improved subthreshold slope an reduced leakage current. This paper deals with various configurations of DG Mosfet such as tied /independent and symmetric/asymmetric gate oxide thickness are explored for ultra low power and high efficient RFID design.

In June 2010, George James T, Saji Joseph, and Vincent Mathew has published a paper entitled "Effect of Counter – doping Thickness on DG Mosfet characteristics ". This paper presents a study of the influence of variation of counter doping thickness on SCE in symmetric DG-Mosfet. Short channel effects are estimated from the computed values of current-voltage characteristics. Two dimensional Quantum transport equation and Poisson Equations are used to compute DG mosfet characteristics.

Again in 2010, Pramod Kumar Tiwari has published a paper entitled " Threshold voltage model for Symmetric DG MOSFET with uniform doping profile." This paper prents a 2- dimensional model for the potential distribution and threshold voltage of symmetric DG MOSFET with a Gaussian doping profile in the vertical direction of the channel.

In 2009, H. Abebe, E. Cumberbatch, H. Morris, V. Tyree, T. Numata and S. Uno has published a paper entitled " Symmetric and Asymmetric DG-Mosfet modeling." In this paper an analytical compact model for the asymmetric lightly doped DG-mosfet is presented. This model is developed using the Lambert Function and a 2-d paraboblic electrostatic potential approximation.

We have gone through all the references above and took them as base papers for our research work and proposed our design.

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